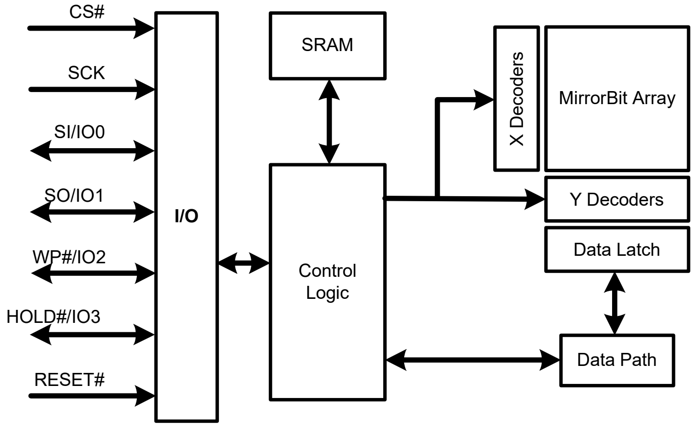
S25FL128S/S25FL256S

128 Mb (16 MB)/256 Mb (32 MB) 3.0V SPI Flash Memory

Features

- CMOS 3.0 Volt Core with Versatile I/O
- SPI with Multi-I/O
  - SPI Clock polarity and phase modes 0 and 3
  - DDR option
  - Extended Addressing: 24- or 32-bit address options
  - Serial Command set and footprint compatible with S25FL-A, S25FL-K, and S25FL-P SPI families
  - Multi I/O Command set and footprint compatible with S25FL-P SPI family
- READ Commands
  - Normal, Fast, Dual, Quad, Fast DDR, Dual DDR, Quad DDR
  - AutoBoot - power up or reset and execute a Normal or Quad read command automatically at a preselected address
  - Common Flash Interface (CFI) data for configuration information.
- Programming (1.5 MBps)
  - 256 or 512 Byte Page Programming buffer options
  - Quad-Input Page Programming (QPP) for slow clock systems
  - Automatic ECC-internal hardware Error Correction Code generation with single bit error correction
- Erase (0.5 to 0.65 MBps)
  - Hybrid sector size option - physical set of thirty two 4-KB sectors at top or bottom of address space with all remaining sectors of 64 KB, for compatibility with prior generation S25-FL devices
  - Uniform sector option - always erase 256-KB blocks for software compatibility with higher density and future devices.
- Cycling Endurance
  - 100,000 Program-Erase Cycles, minimum
- Data Retention
  - 20 Year Data Retention, minimum
- Security features
  - OTP array of 1024 bytes
  - Block Protection:
    - Status Register bits to control protection against program or erase of a contiguous range of sectors.
    - Hardware and software control options
  - Advanced Sector Protection (ASP)
    - Individual sector protection controlled by boot code or password
- Cypress® 65 nm MirrorBit® Technology with Eclipse™ Architecture
- Core Supply Voltage: 2.7V to 3.6V
- I/O Supply Voltage: 1.65V to 3.6V
  - SO16 and FBGA packages
- Temperature Range / Grade:
  - Industrial (–40°C to +85°C)
  - Industrial Plus (–40°C to +105°C)
  - Automotive AEC-Q100 Grade 3 (–40°C to +85°C)
  - Automotive AEC-Q100 Grade 2 (–40°C to +105°C)
  - Automotive AEC-Q100 Grade 1 (–40°C to +125°C)
- Packages (all Pb-free)
  - 16-lead SOIC (300 mil)
  - WSON 6 × 8 mm
  - BGA-24 6 × 8 mm
    - 5 × 5 ball (FAB024) and 4 × 6 ball (FAC024) footprint options
    - Known Good Die (KGD) and Known Tested Die

Logic Block Diagram



Performance Summary

Maximum Read Rates with the Same Core and I/O Voltage ($V_{IO} = V_{CC} = 2.7V$ to $3.6V$)

Command	Clock Rate (MHz)	MBps
Read	50	6.25
Fast Read	133	16.6
Dual Read	104	26
Quad Read	104	52

Maximum Read Rates with Lower I/O Voltage ($V_{IO} = 1.65V$ to $2.7V$, $V_{CC} = 2.7V$ to $3.6V$)

Command	Clock Rate (MHz)	MBps
Read	50	6.25
Fast Read	66	8.25
Dual Read	66	16.5
Quad Read	66	33

Maximum Read Rates DDR ($V_{IO} = V_{CC} = 3V$ to $3.6V$)

Command	Clock Rate (MHz)	MBps
Fast Read DDR	80	20
Dual Read DDR	80	40
Quad Read DDR	80	80

Typical Program and Erase Rates

Operation	KBps
Page Programming (256-byte page buffer - Hybrid Sector Option)	1000
Page Programming (512-byte page buffer - Uniform Sector Option)	1500
4-KB Physical Sector Erase (Hybrid Sector Option)	30
64-KB Physical Sector Erase (Hybrid Sector Option)	500
256-KB Logical Sector Erase (Uniform Sector Option)	500

Current Consumption

Operation	Current (mA)
Serial Read 50 MHz	16 (max)
Serial Read 133 MHz	33 (max)
Quad Read 104 MHz	61 (max)
Quad DDR Read 80 MHz	90 (max)
Program	100 (max)
Erase	100 (max)
Standby	0.07 (typ)

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Hardware Interface

Software Interface

1. Overview

1.1 General Description

The Cypress S25FL128S and S25FL256S devices are flash non-volatile memory products using:

- MirrorBit technology - that stores two data bits in each memory array transistor
- Eclipse architecture - that dramatically improves program and erase performance
- 65 nm process lithography

This family of devices connect to a host system via a SPI. Traditional SPI single bit serial input and output (Single I/O or SIO) is supported as well as optional two bit (Dual I/O or DIO) and four bit (Quad I/O or QIO) serial commands. This multiple width interface is called SPI Multi-I/O or MIO. In addition, the FL-S family adds support for DDR read commands for SIO, DIO, and QIO that transfer address and read data on both edges of the clock.

The Eclipse architecture features a Page Programming Buffer that allows up to 128 words (256 bytes) or 256 words (512 bytes) to be programmed in one operation, resulting in faster effective programming and erase than prior generation SPI program or erase algorithms.

Executing code directly from flash memory is often called Execute-In-Place or XIP. By using FL-S devices at the higher clock rates supported, with QIO or DDR-QIO commands, the instruction read transfer rate can match or exceed traditional parallel interface, asynchronous, NOR flash memories while reducing signal count dramatically.

The S25FL128S and S25FL256S products offer high densities coupled with the flexibility and fast performance required by a variety of embedded applications. They are ideal for code shadowing, XIP, and data storage.

1.2 Migration Notes

1.2.1 Features Comparison

The S25FL128S and S25FL256S devices are command set and footprint compatible with prior generation FL-K and FL-P families.

Table 1. FL Generations Comparison[1, 2, 3, 4, 5]

Parameter	FL-K	FL-P	FL-S
Technology Node	90 nm	90 nm	65 nm
Architecture	Floating Gate	MirrorBit	MirrorBit Eclipse
Release Date	In Production	In Production	2H2011
Density	4 Mb - 128 Mb	32 Mb - 256 Mb	128 Mb - 256 Mb
Bus Width	x1, x2, x4	x1, x2, x4	x1, x2, x4
Supply Voltage	2.7V - 3.6V	2.7V - 3.6V	2.7V - 3.6V / 1.65V - 3.6V V_{IO}
Normal Read Speed (SDR)	6 MBps (50 MHz)	5 MBps (40 MHz)	6 MBps (50 MHz)
Fast Read Speed (SDR)	13 MBps (104 MHz)	13 MBps (104 MHz)	17 MBps (133 MHz)
Dual Read Speed (SDR)	26 MBps (104 MHz)	20 MBps (80 MHz)	26 MBps (104 MHz)
Quad Read Speed (SDR)	52 MBps (104 MHz)	40 MBps (80 MHz)	52 MBps (104 MHz)
Fast Read Speed (DDR)	–	–	20 MBps (80 MHz)
Dual Read Speed (DDR)	–	–	40 MBps (80 MHz)
Quad Read Speed (DDR)	–	–	80 MBps (80 MHz)
Program Buffer Size	256B	256B	256B / 512B
Erase Sector Size	4 KB / 32 KB / 64 KB	64 KB / 256 KB	64 KB / 256 KB
Parameter Sector Size	4 KB	4 KB	4 KB (option)

Notes
1. 256B program page option only for 128-Mb and 256-Mb density FL-S devices.
2. FL-P column indicates FL129P MIO SPI device (for 128-Mb density).
3. 64-KB sector erase option only for 128-Mb/256-Mb density FL-P and FL-S devices.
4. FL-K family devices can erase 4-KB sectors in groups of 32 KB or 64 KB.
5. Refer to individual datasheets for further details.

Table 1. FL Generations Comparison[1, 2, 3, 4, 5] (Continued)

Parameter	FL-K	FL-P	FL-S
Sector Erase Time (typ.)	30 ms (4 KB), 150 ms (64 KB)	500 ms (64 KB)	130 ms (64 KB), 520 ms (256 KB)
Page Programming Time (typ.)	700 µs (256B)	1500 µs (256B)	250 µs (256B), 340 µs (512B)
OTP	768B (3 x 256B)	506B	1024B
Advanced Sector Protection	No	No	Yes
Auto Boot Mode	No	No	Yes
Erase Suspend/Resume	Yes	No	Yes
Program Suspend/Resume	Yes	No	Yes
Operating Temperature	–40°C to +85°C	–40°C to +85°C / +105°C	–40°C to +85°C / +105°C / +125°C

Notes
1. 256B program page option only for 128-Mb and 256-Mb density FL-S devices.
2. FL-P column indicates FL129P MIO SPI device (for 128-Mb density).
3. 64-KB sector erase option only for 128-Mb/256-Mb density FL-P and FL-S devices.
4. FL-K family devices can erase 4-KB sectors in groups of 32 KB or 64 KB.
5. Refer to individual datasheets for further details.

1.2.2 Known Differences from Prior Generations

1.2.2.1 Error Reporting

Prior generation FL memories either do not have error status bits or do not set them if program or erase is attempted on a protected sector. The FL-S family does have error reporting status bits for program and erase operations. These can be set when there is an internal failure to program or erase or when there is an attempt to program or erase a protected sector. In either case, the program or erase operation did not complete as requested by the command.

1.2.2.2 Secure Silicon Region (OTP)

The size and format (address map) of the OTP area is different from prior generations. The method for protecting each portion of the OTP area is different. For additional details, see Section 8.1 Secure Silicon Region (OTP) on page 58.

1.2.2.3 Configuration Register Freeze Bit

The Configuration Register Freeze bit CR1[0], locks the state of the Block Protection bits as in prior generations. In the FL-S family, it also locks the state of the Configuration Register TBPARM bit CR1[2], TBPROT bit CR1[5], and the Secure Silicon Region (OTP) area.

1.2.2.4 Sector Erase Commands

The command for erasing an 8-KB area (two 4-KB sectors) is not supported.

The command for erasing a 4-KB sector is supported only in the 128-Mb and 256-Mb density FL-S devices and only for use on the thirty two 4-KB parameter sectors at the top or bottom of the device address space.

The erase command for 64-KB sectors are supported for the 128-Mb and 256-Mb density FL-S devices when the ordering option for 4-KB parameter sectors with 64-KB uniform sectors are used. The 64-KB erase command may be applied to erase a group of sixteen 4-KB sectors.

The erase command for a 256-KB sector replaces the 64-KB erase command when the ordering option for 256-KB uniform sectors is used for the 128-Mb and 256-Mb density FL-S devices.

1.2.2.5 Deep Power Down

The Deep Power Down (DPD) function is not supported in FL-S family devices.

The legacy DPD (B9h) command code is instead used to enable legacy SPI memory controllers, that can issue the former DPD command, to access a new bank address register. The bank address register allows SPI memory controllers that do not support more than 24 bits of address, the ability to provide higher order address bits for commands, as needed to access the larger address space of the 256-Mb density FL-S device. For additional information, see Section 7.1.1 Extended Address on page 45.

1.2.2.6 New Features

The FL-S family introduces several new features to SPI category memories:

- Extended address for access to higher memory density.
- AutoBoot for simpler access to boot code following power up.
- Enhanced High Performance read commands using mode bits to eliminate the overhead of SIO instructions when repeating the same type of read command.
- Multiple options for initial read latency (number of dummy cycles) for faster initial access time or higher clock rate read commands.
- DDR read commands for SIO, DIO, and QIO.
- Automatic ECC for enhanced data integrity.
- Advanced Sector Protection for individually controlling the protection of each sector. This is very similar to the Advanced Sector Protection feature found in several other Cypress parallel interface NOR memory families.

1.3 Glossary

Command	All information transferred between the host system and memory during one period while CS# is LOW. This includes the instruction (sometimes called an operation code or opcode) and any required address, mode bits, latency cycles, or data.
DDP **(Dual Die Package)**	Two die stacked within the same package to increase the memory capacity of a single package. Often also referred to as a Multi-Chip Package (MCP).
DDR **(Double Data Rate)**	When input and output are latched on every edge of SCK.
ECC	ECC Unit = 16 byte aligned and length data groups in the main Flash array and OTP array, each of which has its own hidden ECC syndrome to enable error correction on each group.
Flash	The name for a type of EEPROM that erases large blocks of memory bits in parallel, making the erase operation much faster than early EEPROM.
High	A signal voltage level $\geq V_{IH}$ or a logic level representing a binary one (1).
Instruction	The 8 bit code indicating the function to be performed by a command (sometimes called an operation code or opcode). The instruction is always the first 8 bits transferred from host system to the memory in any command.
Low	A signal voltage level $\leq V_{IL}$ or a logic level representing a binary zero (0).
LSb **(Least Significant Bit)**	The right most bit, with the lowest order of magnitude value, within a group of bits of a register or data value.
MSb **(Most Significant Bit)**	The left most bit, with the highest order of magnitude value, within a group of bits of a register or data value.
LSB **(Least Significant Byte)**	The right most byte, within a group of bytes.
MSB **(Most Significant Byte)**	The left most bit, within a group of bytes
Non-Volatile	No power is needed to maintain data stored in the memory.
OPN **(Ordering Part Number)**	The alphanumeric string specifying the memory device type, density, package, factory non-volatile configuration, etc. used to select the desired device.

Page	512 bytes or 256 bytes aligned and length group of data. The size assigned for a page depends on the Ordering Part Number.
PCB	Printed Circuit Board
PPAP	Production Part Approval Process
Register Bit References	Are in the format: Register_name[bit_number] or Register_name[bit_range_MSb: bit_range_LSB]
SDR (Single Data Rate)	When input is latched on the rising edge and output on the falling edge of SCK.
Sector	Erase unit size; depending on device model and sector location this may be 4 KB, 64 KB or 256 KB.
Write	An operation that changes data within volatile or nonvolatile registers bits or nonvolatile flash memory. When changing nonvolatile data, an erase and reprogramming of any unchanged nonvolatile data is done, as part of the operation, such that the nonvolatile data is modified by the write operation, in the same way that volatile data is modified – as a single operation. The nonvolatile data appears to the host system to be updated by the single write command, without the need for separate commands for erase and reprogram of adjacent, but unaffected data.

1.4 Other Resources

1.4.1 Cypress Flash Memory Roadmap

www.cypress.com/product-roadmaps/cypress-flash-memory-roadmap

1.4.2 Links to Software

www.cypress.com/software-and-drivers-cypress-flash-memory

1.4.3 Links to Application Notes

www.cypress.com/appnotes

Hardware Interface

Serial Peripheral Interface with Multiple Input / Output (SPI-MIO)
Many memory devices connect to their host system with separate parallel control, address, and data signals that require a large number of signal connections and larger package size. The large number of connections increase power consumption due to so many signals switching and the larger package increases cost.

The S25FL128S and S25FL256S devices reduce the number of signals for connection to the host system by serially transferring all control, address, and data information over 4 to 6 signals. This reduces the cost of the memory package, reduces signal switching power, and either reduces the host connection count or frees host connectors for use in providing other features.

The S25FL128S and S25FL256S devices use the industry standard single bit Serial Peripheral Interface (SPI) and also supports optional extension commands for two bit (Dual) and four bit (Quad) wide serial transfers. This multiple width interface is called SPI Multi-I/O or SPI-MIO.

2. Signal Descriptions

2.1 Input/Output Summary

Table 2. Signal List

Signal Name	Type	Description
RESET#	Input	**Hardware Reset:** Low = device resets and returns to Standby state, ready to receive a command. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used.
SCK	Input	**Serial Clock**
CS#	Input	**Chip Select**
SI / IO0	I/O	**Serial Input** for single bit data commands or IO0 for Dual or Quad commands.
SO / IO1	I/O	**Serial Output** for single bit data commands. IO1 for Dual or Quad commands.
WP# / IO2	I/O	**Write Protect** when not in Quad mode. IO2 in Quad mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
HOLD# / IO3	I/O	**Hold** (pause) serial transfer in single bit or Dual data commands. IO3 in Quad-I/O mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
V_{CC}	Supply	**Core Power Supply.**
V_{IO}	Supply	**Versatile I/O Power Supply.**
V_{SS}	Supply	**Ground.**
NC	Unused	**Not Connected.** No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a PCB. However, any signal connected to an NC must not have voltage levels higher than V_{IO}.
RFU	Reserved	**Reserved for Future Use.** No device internal signal is currently connected to the package connector but there is potential future use of the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.
DNU	Reserved	**Do Not Use.** A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to this connection.

2.2 Address and Data Configuration

Traditional SPI single bit wide commands (Single or SIO) send information from the host to the memory only on the SI signal. Data may be sent back to the host serially on the Serial Output (SO) signal.

Dual or Quad Output commands send information from the host to the memory only on the SI signal. Data will be returned to the host as a sequence of bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

Dual or Quad Input/Output (I/O) commands send information from the host to the memory as bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

2.3 RESET#

The RESET# input provides a hardware method of resetting the device to standby state, ready for receiving a command. When RESET# is driven to logic LOW (V_{IL}) for at least a period of t_{RP}, the device:

- terminates any operation in progress,
- tristates all outputs,
- resets the volatile bits in the Configuration Register,
- resets the volatile bits in the Status Registers,
- resets the Bank Address Register to zero,
- loads the Program Buffer with all ones,
- reloads all internal configuration information necessary to bring the device to standby mode,
- and resets the internal Control Unit to Standby state.

RESET# causes the same initialization process as is performed when power comes up and requires t_{PU} time.

RESET# may be asserted LOW at any time. To ensure data integrity, any operation that was interrupted by a hardware reset should be reinitiated once the device is ready to accept a command sequence.

When RESET# is first asserted LOW, the device draws I_{CC1} (50 MHz value) during t_{PU}. If RESET# continues to be held at V_{SS}, the device draws CMOS standby current (I_{SB}).

RESET# has an internal pull-up resistor and may be left unconnected in the host system if not used.

The RESET# input is not available on all packages options. When not available, the RESET# input of the device is tied to the inactive state, inside the package.

2.4 Serial Clock (SCK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCK signal. Data output changes after the falling edge of SCK, in SDR commands, and after every edge in DDR commands.

2.5 Chip Select (CS#)

The chip select signal indicates when a command for the device is in process and the other signals are relevant for the memory device. When the CS# signal is at the logic HIGH state, the device is not selected and all input signals are ignored and all output signals are high impedance. Unless an internal Program, Erase or Write Registers (WRR) embedded operation is in progress, the device will be in the Standby Power mode. Driving the CS# input to logic LOW state enables the device, placing it in the Active Power mode. After Power-up, a falling edge on CS# is required prior to the start of any command.

2.6 Serial Input (SI) / IO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCK clock signal.

SI becomes IO0 - an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

2.7 Serial Output (SO) / IO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCK clock signal.

SO becomes IO1 - an input and output during Dual and Quad commands for receiving addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

2.8 Write Protect (WP#) / IO2

When WP# is driven LOW (V_{IL}), during a WRR command and while the Status Register Write Disable (SRWD) bit of the Status Register is set to a ‘1’, it is not possible to write to the Status and Configuration Registers. This prevents any alteration of the Block Protect (BP2, BP1, BP0) and TBPROT bits of the Status Register. As a consequence, all the data bytes in the memory area that are protected by the Block Protect and TBPROT bits, are also hardware protected against data modification if WP# is LOW during a WRR command.

The WP# function is not available when the Quad mode is enabled (CR[1]=1). The WP# function is replaced by IO2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

WP# has an internal pull-up resistor; when unconnected, WP# is at V_{IH} and may be left unconnected in the host system if not used for Quad mode.

2.9 Hold (HOLD#) / IO3

The Hold (HOLD#) signal is used to pause any serial communications with the device without deselecting the device or stopping the serial clock.

To enter the Hold condition, the device must be selected by driving the CS# input to the logic LOW state. It is recommended that the user keep the CS# input LOW state during the entire duration of the Hold condition. This is to ensure that the state of the interface logic remains unchanged from the moment of entering the Hold condition. If the CS# input is driven to the logic HIGH state while the device is in the Hold condition, the interface logic of the device will be reset. To restart communication with the device, it is necessary to drive HOLD# to the logic HIGH state while driving the CS# signal into the logic LOW state. This prevents the device from going back into the Hold condition.

The Hold condition starts on the falling edge of the Hold (HOLD#) signal, provided that this coincides with SCK being at the logic LOW state. If the falling edge does not coincide with the SCK signal being at the logic LOW state, the Hold condition starts whenever the SCK signal reaches the logic LOW state. Taking the HOLD# signal to the logic LOW state does not terminate any Write, Program or Erase operation that is currently in progress.

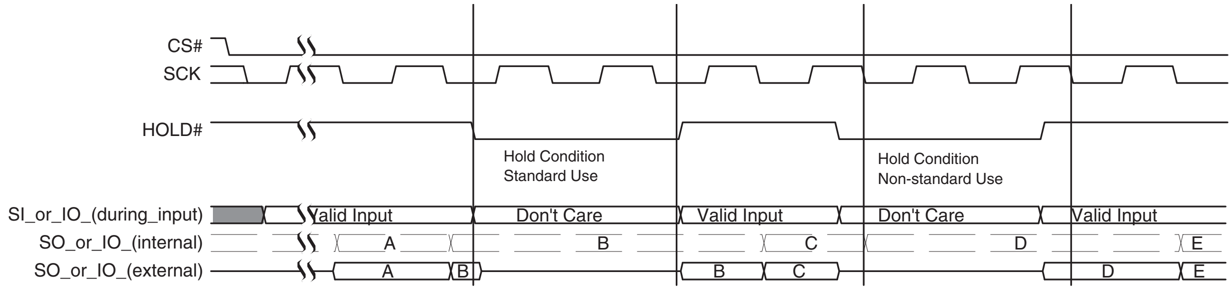
During the Hold condition, SO is in high impedance and both the SI and SCK input are Don't Care.

The Hold condition ends on the rising edge of the Hold (HOLD#) signal, provided that this coincides with the SCK signal being at the logic LOW state. If the rising edge does not coincide with the SCK signal being at the logic LOW state, the Hold condition ends whenever the SCK signal reaches the logic LOW state.

The HOLD# function is not available when the Quad mode is enabled (CR1[1] =1). The Hold function is replaced by IO3 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

The HOLD# signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad mode.

Figure 1. HOLD Mode Operation



2.10 Core Voltage Supply (V_{CC})

V_{CC} is the voltage source for all device internal logic. It is the single voltage used for all device internal functions including read, program, and erase. The voltage may vary from 2.7V to 3.6V.

2.11 Versatile I/O Power Supply (V_{IO})

The Versatile I/O (V_{IO}) supply is the voltage source for all device input receivers and output drivers and allows the host system to set the voltage levels that the device tolerates on all inputs and drives on outputs (address, control, and IO signals). The V_{IO} range is 1.65V to V_{CC}. V_{IO} cannot be greater than V_{CC}.

For example, a V_{IO} of 1.65V - 3.6V allows for I/O at the 1.8V, 2.5V or 3V levels, driving and receiving signals to and from other 1.8V, 2.5V or 3V devices on the same data bus. V_{IO} may be tied to V_{CC} so that interface signals operate at the same voltage as the core of the device. V_{IO} is not available in all package options, when not available the V_{IO} supply is tied to V_{CC} internal to the package.

During the rise of power supplies, the V_{IO} supply voltage must remain less than or equal to the V_{CC} supply voltage. This supply is not available in all package options. For a backward compatible with the SO16 package, the V_{IO} supply is tied to V_{CC} inside the package; thus, the IO will function at V_{CC} level.

2.12 Supply and Signal Ground (V_{SS})

V_{SS} is the common voltage drain and ground reference for the device core, input signal receivers, and output drivers.

2.13 Not Connected (NC)

No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a PCB. However, any signal connected to an NC must not have voltage levels higher than V_{IO}.

2.14 Reserved for Future Use (RFU)

No device internal signal is currently connected to the package connector but is there potential future use of the connector. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.

2.15 Do Not Use (DNU)

A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.

2.16 Block Diagrams

Figure 2. Bus Master and Memory Devices on the SPI Bus - Single Bit Data Path

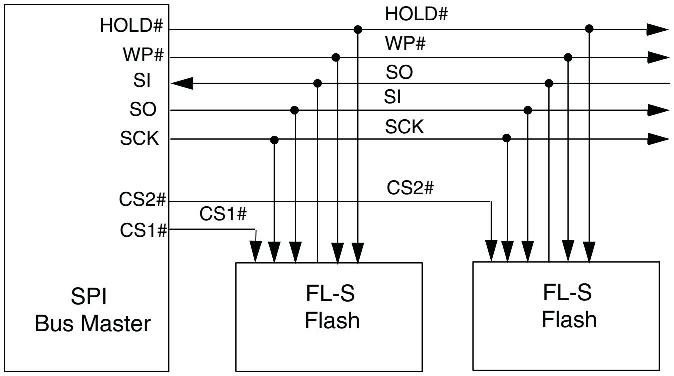


Figure 3. Bus Master and Memory Devices on the SPI Bus - Dual Bit Data Path

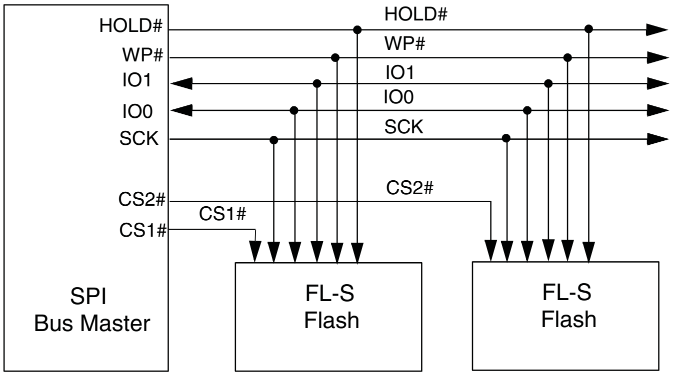
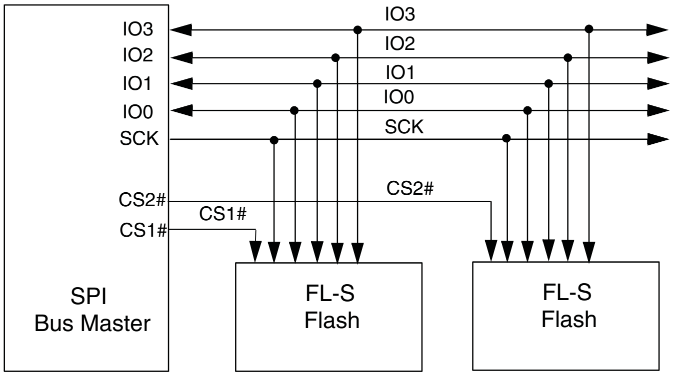


Figure 4. Bus Master and Memory Devices on the SPI Bus - Quad Bit Data Path



3. Signal Protocols

3.1 SPI Clock Modes

3.1.1 SDR

The S25FL128S and S25FL256S devices can be driven by an embedded microcontroller (bus master) in either of the two following clocking modes.

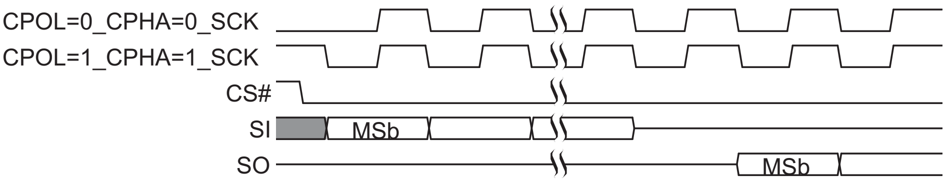
- **Mode 0** with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0
- **Mode 3** with CPOL = 1 and, CPHA = 1

For these two modes, input data into the device is always latched in on the rising edge of the SCK signal and the output data is always available from the falling edge of the SCK clock signal.

The difference between the two modes is the clock polarity when the bus master is in Standby mode and not transferring any data.

- SCK will stay at logic LOW state with CPOL = 0, CPHA = 0
- SCK will stay at logic HIGH state with CPOL = 1, CPHA = 1

Figure 5. SPI SDR Modes Supported



Timing diagrams throughout the remainder of the document are generally shown as both mode 0 and 3 by showing SCK as both HIGH and LOW at the fall of CS#. In some cases, a timing diagram may show only mode 0 with SCK LOW at the fall of CS#. In such a case, mode 3 timing simply means clock is HIGH at the fall of CS# so no SCK rising edge set up or hold time to the falling edge of CS# is needed for mode 3.

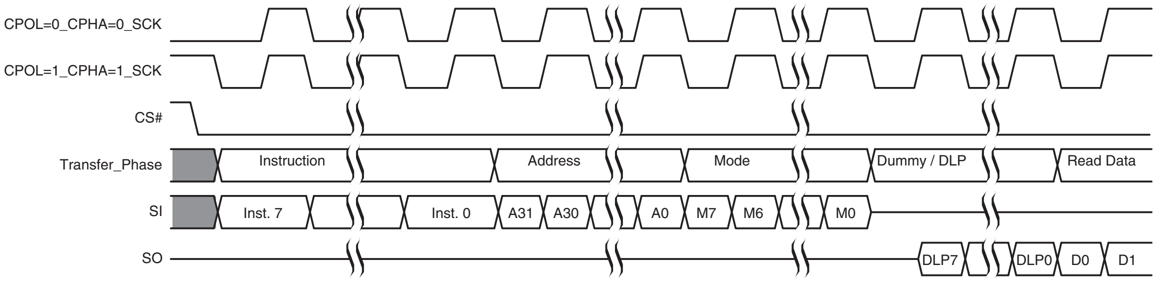
SCK cycles are measured (counted) from one falling edge of SCK to the next falling edge of SCK. In mode 0 the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already low at the beginning of a command.

3.1.2 DDR

Mode 0 and Mode 3 are also supported for DDR commands. In DDR commands, the instruction bits are always latched on the rising edge of clock, the same as in SDR commands. However, the address and input data that follow the instruction are latched on both the rising and falling edges of SCK. The first address bit is latched on the first rising edge of SCK following the falling edge at the end of the last instruction bit. The first bit of output data is driven on the falling edge at the end of the last access latency (dummy) cycle.

SCK cycles are measured (counted) in the same way as in SDR commands, from one falling edge of SCK to the next falling edge of SCK. In mode 0 the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already low at the beginning of a command.

Figure 6. SPI DDR Modes Supported



3.2 Command Protocol

All communication between the host system and S25FL128S and S25FL256S memory devices is in the form of units called commands.

All commands begin with an instruction that selects the type of information transfer or device operation to be performed. Commands may also have an address, instruction modifier, latency period, data transfer to the memory, or data transfer from the memory. All instruction, address, and data information is transferred serially between the host system and memory device.

All instructions are transferred from host to memory as a single bit serial sequence on the SI signal.

Single bit wide commands may provide an address or data sent only on the SI signal. Data may be sent back to the host serially on the SO signal.

Dual or Quad Output commands provide an address sent to the memory only on the SI signal. Data will be returned to the host as a sequence of bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

Dual or Quad Input/Output (I/O) commands provide an address sent from the host as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3.

Commands are structured as follows:

- Each command begins with CS# going LOW and ends with CS# returning HIGH. The memory device is selected by the host driving the Chip Select (CS#) signal low throughout a command.
- The serial clock (SCK) marks the transfer of each bit or group of bits between the host and memory.
- Each command begins with an eight bit (byte) instruction. The instruction is always presented only as a single bit serial sequence on the Serial Input (SI) signal with one bit transferred to the memory device on each SCK rising edge. The instruction selects the type of information transfer or device operation to be performed.
- The instruction may be stand alone or may be followed by address bits to select a location within one of several address spaces in the device. The instruction determines the address space used. The address may be either a 24-bit or a 32-bit byte boundary, address. The address transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- The width of all transfers following the instruction are determined by the instruction sent. Following transfers may continue to be single bit serial on only the SI or Serial Output (SO) signals, they may be done in two bit groups per (dual) transfer on the IO0 and IO1 signals, or they may be done in 4 bit groups per (quad) transfer on the IO0-IO3 signals. Within the dual or quad groups the least significant bit is on IO0. More significant bits are placed in significance order on each higher numbered IO signal. SIngle bits or parallel bit groups are transferred in most to least significant bit order.
- Some instructions send an instruction modifier called mode bits, following the address, to indicate that the next command will be of the same type with an implied, rather than an explicit, instruction. The next command thus does not provide an instruction byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands. The mode bit transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- The address or mode bits may be followed by write data to be stored in the memory device or by a read latency period before read data is returned to the host.
- Write data bit transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- SCK continues to toggle during any read access latency period. The latency may be zero to several SCK cycles (also referred to as dummy cycles). At the end of the read latency cycles, the first read data bits are driven from the outputs on SCK falling edge at the end of the last read latency cycle. The first read data bits are considered transferred to the host on the following SCK rising edge. Each following transfer occurs on the next SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- If the command returns read data to the host, the device continues sending data transfers until the host takes the CS# signal HIGH. The CS# signal can be driven HIGH after any transfer in the read data sequence. This will terminate the command.
- At the end of a command that does not return data, the host drives the CS# input HIGH. The CS# signal must go HIGH after the eighth bit, of a stand alone instruction or, of the last write data byte that is transferred. That is, the CS# signal must be driven HIGH when the number of clock cycles after CS# signal was driven LOW is an exact multiple of eight cycles. If the CS# signal does not go HIGH exactly at the eight SCK cycle boundary of the instruction or write data, the command is rejected and not executed.
- All instruction, address, and mode bits are shifted into the device with the Most Significant Bits (MSb) first. The data bits are shifted in and out of the device MSb first. All data is transferred in byte units with the lowest address byte sent first. Following bytes of data are sent in lowest to highest byte address order i.e. the byte address increments.

- All attempts to read the flash memory array during a program, erase, or a write cycle (embedded operations) are ignored. The embedded operation will continue to execute without any affect. A very limited set of commands are accepted during an embedded operation. These are discussed in the individual command descriptions.
- Depending on the command, the time for execution varies. A command to read status information from an executing command is available to determine when the command completes execution and whether the command was successful.

3.2.1 Command Sequence Examples

Figure 7. Standalone Instruction Command

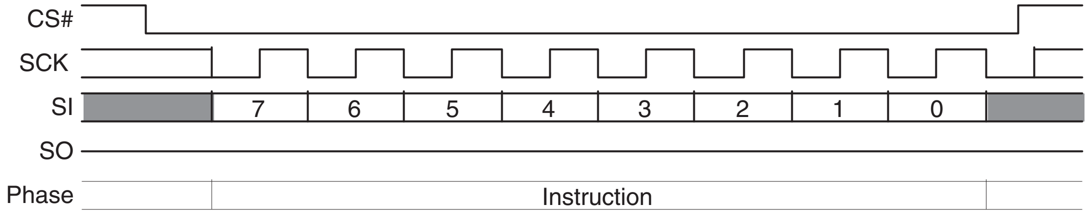


Figure 8. Single Bit Wide Input Command

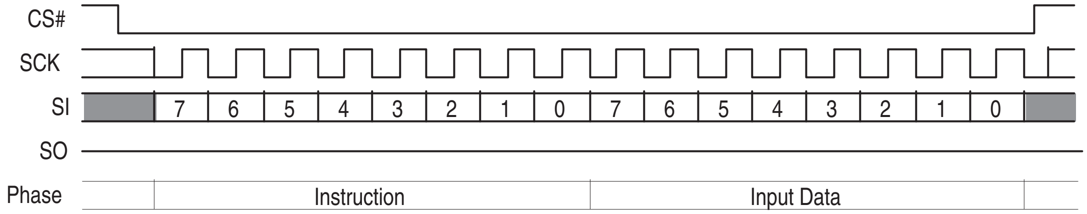


Figure 9. Single Bit Wide Output Command

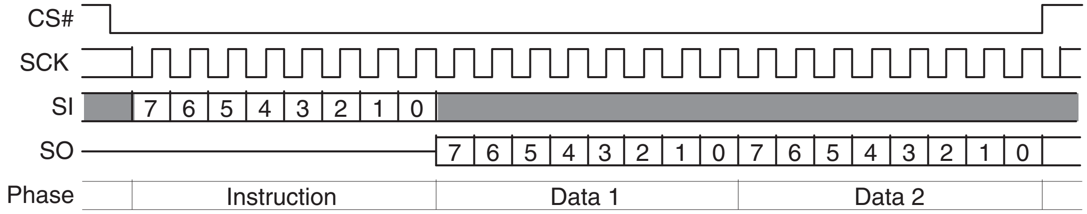


Figure 10. Single Bit Wide I/O Command without Latency

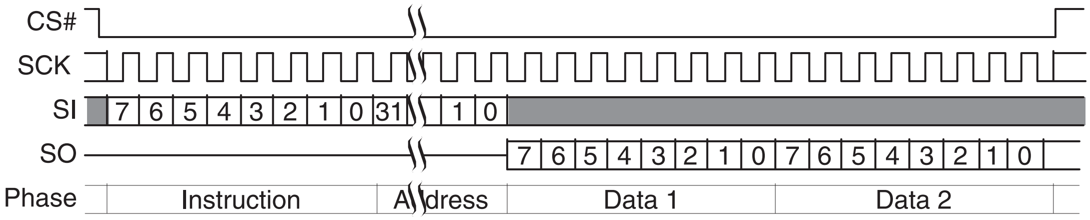


Figure 11. Single Bit Wide I/O Command with Latency

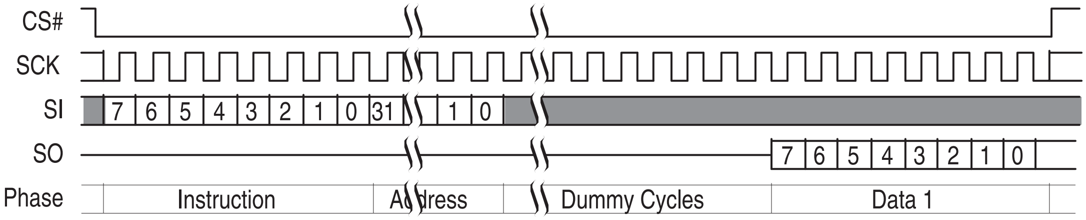


Figure 12. Dual Output Command

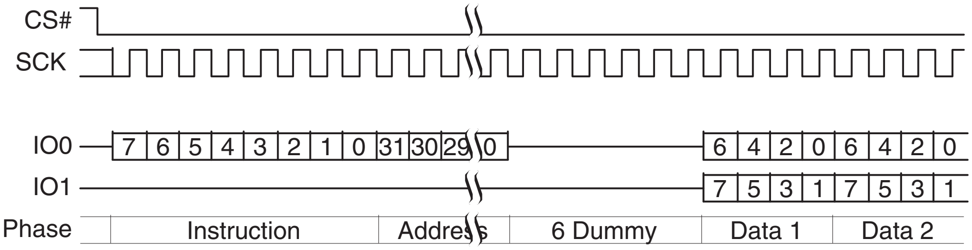


Figure 13. Quad Output Command without Latency

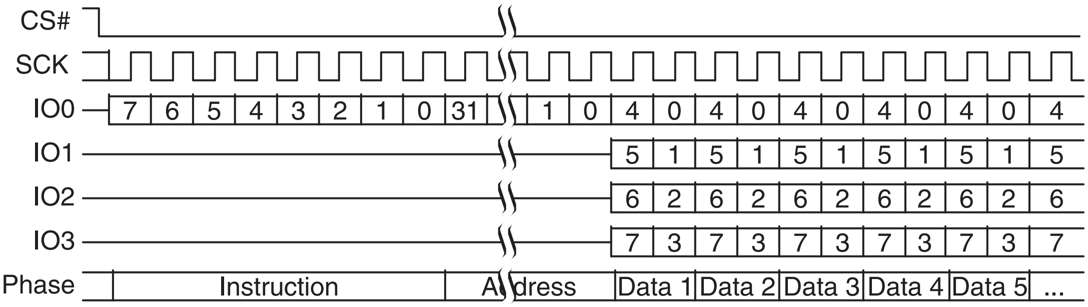


Figure 14. Dual I/O Command

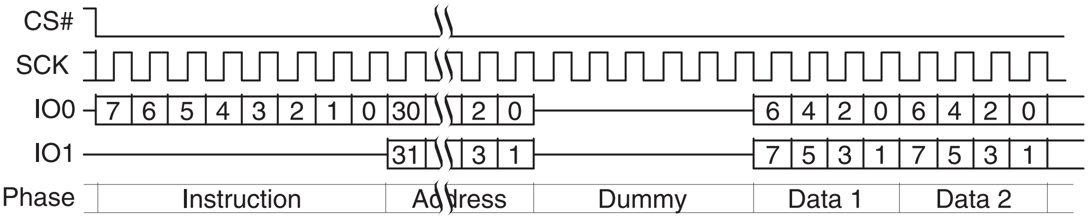


Figure 15. Quad I/O Command

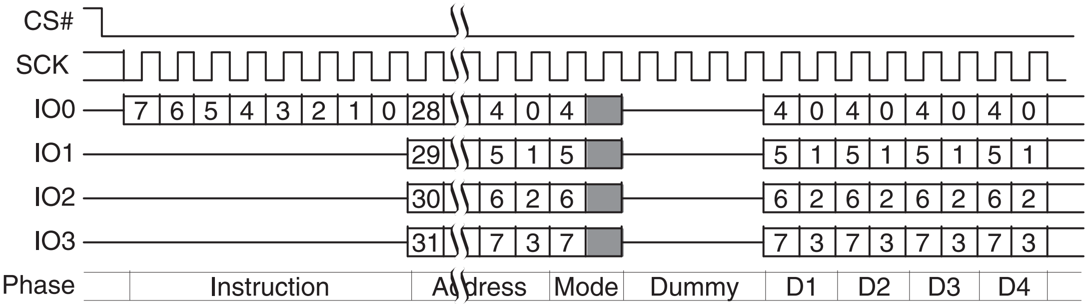


Figure 16. DDR Fast Read with EHPLC = 00b

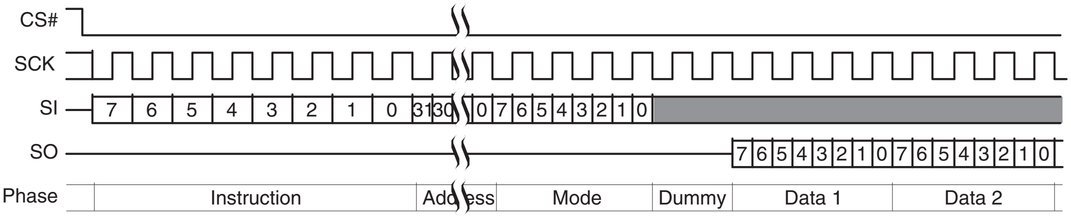


Figure 17. DDR Dual I/O Read with EHPLC = 01b and DLP

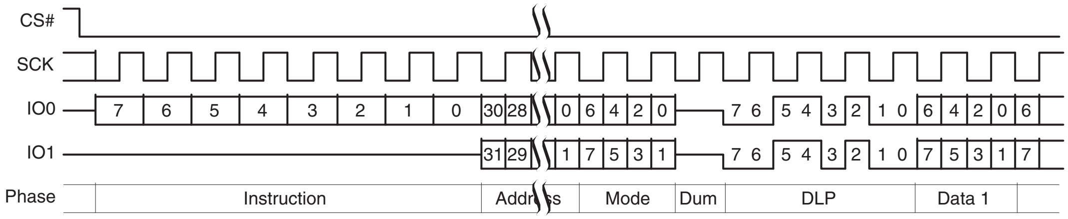
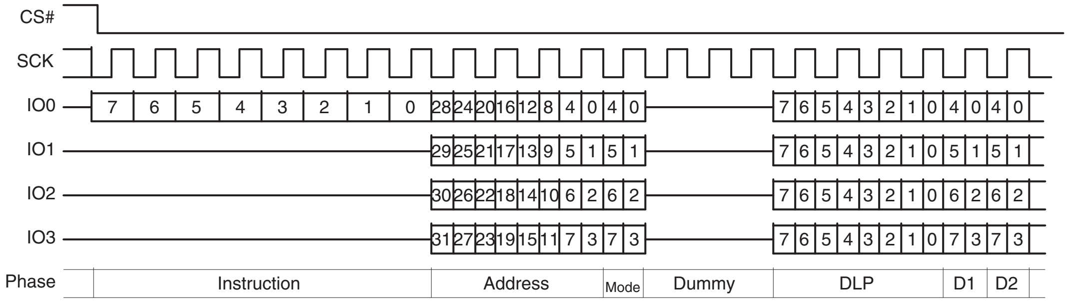


Figure 18. DDR Quad I/O Read



Additional sequence diagrams, specific to each command, are provided in Section 9. Commands on page 64.

3.3 Interface States

This section describes the input and output signal levels as related to the SPI interface behavior.

Table 3. Interface States Summary

Interface State	V_{CC}	V_{IO}	RESET#	SCK	CS#	HOLD# / IO3	WP# / IO2	SO / IO1	SI / IO0
Power-Off	< V_{CC} (low)	≤ V_{CC}	X	X	X	X	X	Z	X
Low Power Hardware Data Protection	< V_{CC} (cut-off)	≤ V_{CC}	X	X	X	X	X	Z	X
Power-On (Cold) Reset	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	X	X	X	X	X	Z	X
Hardware (Warm) Reset	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HL	X	X	X	X	Z	X
Interface Standby	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	X	HH	X	X	Z	X
Instruction Cycle	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HH	HV	Z	HV
Hold Cycle	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HV or HT	HL	HL	X	X	X
Single Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HH	X	Z	HV
Single Latency (Dummy) Cycle	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HH	X	Z	X
Single Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HH	X	MV	X
Dual Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HH	X	HV	HV
Dual Latency (Dummy) Cycle	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HH	X	X	X
Dual Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HH	X	MV	MV
QPP Address Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	X	X	X	HV
Quad Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HV	HV	HV	HV

Table 3. Interface States Summary (Continued)

Interface State	V_{CC}	V_{IO}	RESET #	SCK	CS#	HOLD# / IO3	WP# / IO2	SO / IO1	SI / IO0
Quad Latency (Dummy) Cycle	$\geq V_{CC}$ (min)	$\geq V_{IO}$ (min) $\leq V_{CC}$	HH	HT	HL	X	X	X	X
Quad Output Cycle Memory to Host Transfer	$\geq V_{CC}$ (min)	$\geq V_{IO}$ (min) $\leq V_{CC}$	HH	HT	HL	MV	MV	MV	MV
DDR Single Input Cycle Host to Memory Transfer	$\geq V_{CC}$ (min)	$\geq V_{IO}$ (min) $\leq V_{CC}$	HH	HT	HL	X	X	X	HV
DDR Dual Input Cycle Host to Memory Transfer	$\geq V_{CC}$ (min)	$\geq V_{IO}$ (min) $\leq V_{CC}$	HH	HT	HL	X	X	HV	HV
DDR Quad Input Cycle Host to Memory Transfer	$\geq V_{CC}$ (min)	$\geq V_{IO}$ (min) $\leq V_{CC}$	HH	HT	HL	HV	HV	HV	HV
DDR Latency (Dummy) Cycle	$\geq V_{CC}$ (min)	$\geq V_{IO}$ (min) $\leq V_{CC}$	HH	HT	HL	MV or Z	MV or Z	MV or Z	MV or Z
DDR Single Output Cycle Memory to Host Transfer	$\geq V_{CC}$ (min)	$\geq V_{IO}$ (min) $\leq V_{CC}$	HH	HT	HL	Z	Z	MV	X
DDR Dual Output Cycle Memory to Host Transfer	$\geq V_{CC}$ (min)	$\geq V_{IO}$ (min) $\leq V_{CC}$	HH	HT	HL	Z	Z	MV	MV
DDR Quad Output Cycle Memory to Host Transfer	$\geq V_{CC}$ (min)	$\geq V_{IO}$ (min) $\leq V_{CC}$	HH	HT	HL	MV	MV	MV	MV

Legend
Z = No driver - floating signal
HL = Host driving V_{IL}
HH = Host driving V_{IH}
HV = Either HL or HH
X = HL or HH or Z
HT = Toggling between HL and HH
ML = Memory driving V_{IL}
MH = Memory driving V_{IH}
MV = Either ML or MH

3.3.1 Power-Off

When the core supply voltage is at or below the V_{CC} (low) voltage, the device is considered to be powered off. The device does not react to external signals, and is prevented from performing any program or erase operation.

3.3.2 Low Power Hardware Data Protection

When V_{CC} is less than V_{CC} (cut-off) the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

3.3.3 Power-On (Cold) Reset

When the core voltage supply remains at or below the V_{CC} (low) voltage for $\geq t_{PD}$ time, then rises to $\geq V_{CC\ (Minimum)}$ the device will begin its Power-On Reset (POR) process. POR continues until the end of t_{PU}. During t_{PU}, the device does not react to external input signals nor drive any outputs. Following the end of t_{PU}, the device transitions to the Interface Standby state and can accept commands. For additional information on POR, see Section 5.3.1 Power-On (Cold) Reset on page 29.

3.3.4 Hardware (Warm) Reset

Some of the device package options provide a RESET# input. When RESET# is driven LOW for t_{RP} time, the device starts the hardware reset process. The process continues for t_{RPH} time. Following the end of both t_{RPH} and the reset hold time following the rise of RESET# (t_{RH}) the device transitions to the Interface Standby state and can accept commands. For additional information on hardware reset, see Section 28 POR followed by Hardware Reset on page 29.

3.3.5 Interface Standby

When CS# is HIGH, the SPI interface is in Standby state. Inputs other than RESET# are ignored. The interface waits for the beginning of a new command. The next interface state is Instruction Cycle when CS# goes LOW to begin a new command.

While in interface Standby state, the memory device draws standby current (I_{SB}) if no embedded algorithm is in progress. If an embedded algorithm is in progress, the related current is drawn until the end of the algorithm when the entire device returns to standby current draw.

3.3.6 Instruction Cycle

When the host drives the MSb of an instruction and CS# goes LOW, on the next rising edge of SCK the device captures the MSb of the instruction that begins the new command. On each following rising edge of SCK, the device captures the next lower significance bit of the 8-bit instruction. The host keeps RESET# HIGH, CS# LOW, HOLD# HIGH, and drives Write Protect (WP#) signal as needed for the instruction. However, WP# is only relevant during instruction cycles of a WRR command and is otherwise ignored.

Each instruction selects the address space that is operated on and the transfer format used during the remainder of the command. The transfer format may be Single, Dual output, Quad output, Dual I/O, Quad I/O, DDR Single I/O, DDR Dual I/O, or DDR Quad I/O. The expected next interface state depends on the instruction received.

Some commands are standalone, needing no address or data transfer to or from the memory. The host returns CS# HIGH after the rising edge of SCK for the eighth bit of the instruction in such commands. The next interface state in this case is Interface Standby.

3.3.7 Hold

When Quad mode is not enabled (CR[1]=0), the HOLD# / IO3 signal is used as the HOLD# input. The host keeps RESET# HIGH, HOLD# LOW, SCK may be at a valid level or continue toggling, and CS# is LOW. When HOLD# is LOW a command is paused, as though SCK were held LOW. SI / IO0 and SO / IO1 ignore the input level when acting as inputs and are high impedance when acting as outputs during Hold state. Whether these signals are input or output depends on the command and the point in the command sequence when HOLD# is asserted LOW.

When HOLD# returns HIGH, the next state is the same state the interface was in just before HOLD# was asserted LOW.

When Quad mode is enabled, the HOLD# / IO3 signal is used as IO3.

During DDR commands, the HOLD# and WP# inputs are ignored.

3.3.8 Single Input Cycle - Host to Memory Transfer

Several commands transfer information after the instruction on the single serial input (SI) signal from host to the memory device. The dual output, and quad output commands send address to the memory using only SI but return read data using the I/O signals. The host keeps RESET# HIGH, CS# LOW, HOLD# HIGH, and drives SI as needed for the command. The memory does not drive the Serial Output (SO) signal.

The expected next interface state depends on the instruction. Some instructions continue sending address or data to the memory using additional Single Input Cycles. Others may transition to Single Latency, or directly to Single, Dual, or Quad Output.

3.3.9 Single Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR[7:6]). During the latency cycles, the host keeps RESET# HIGH, CS# LOW, and HOLD# HIGH. The Write Protect (WP#) signal is ignored. The host may drive the SI signal during these cycles or the host may leave SI floating. The memory does not use any data driven on SI / I/O0 or other I/O signals during the latency cycles. In dual or quad read commands, the host must stop driving the I/O signals on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving I/O signals during latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the Serial Output (SO) or I/O signals during the latency cycles.

The next interface state depends on the command structure i.e., the number of latency cycles, and whether the read is single, dual, or quad width.

3.3.10 Single Output Cycle - Memory to Host Transfer

Several commands transfer information back to the host on the single Serial Output (SO) signal. The host keeps RESET# HIGH, CS# LOW, and HOLD# HIGH. The Write Protect (WP#) signal is ignored. The memory ignores the Serial Input (SI) signal. The memory drives SO with data.

The next interface state continues to be Single Output Cycle until the host returns CS# to HIGH ending the command.

3.3.11 Dual Input Cycle - Host to Memory Transfer

The Read Dual I/O command transfers two address or mode bits to the memory in each cycle. The host keeps RESET# HIGH, CS# LOW, HOLD# HIGH. The Write Protect (WP#) signal is ignored. The host drives address on SI / IO0 and SO / IO1.

The next interface state following the delivery of address and mode bits is a Dual Latency Cycle if there are latency cycles needed or Dual Output Cycle if no latency is required.

3.3.12 Dual Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the Configuration Register (CR[7:6]). During the latency cycles, the host keeps RESET# HIGH, CS# LOW, and HOLD# HIGH. The Write Protect (WP#) signal is ignored. The host may drive the SI / IO0 and SO / IO1 signals during these cycles or the host may leave SI / IO0 and SO / IO1 floating. The memory does not use any data driven on SI / IO0 and SO / IO1 during the latency cycles. The host must stop driving SI / IO0 and SO / IO1 on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the SI / IO0 and SO / IO1 signals during the latency cycles.

The next interface state following the last latency cycle is a Dual Output Cycle.

3.3.13 Dual Output Cycle - Memory to Host Transfer

The Read Dual Output and Read Dual I/O return data to the host two bits in each cycle. The host keeps RESET# HIGH, CS# LOW, and HOLD# HIGH. The Write Protect (WP#) signal is ignored. The memory drives data on the SI / IO0 and SO / IO1 signals during the dual output cycles.

The next interface state continues to be Dual Output Cycle until the host returns CS# to HIGH ending the command.

3.3.14 QPP or QOR Address Input Cycle

The Quad Page Program and Quad Output Read commands send address to the memory only on IO0. The other IO signals are ignored because the device must be in Quad mode for these commands thus the Hold and Write Protect features are not active. The host keeps RESET# HIGH, CS# LOW, and drives IO0.

For QPP the next interface state following the delivery of address is the Quad Input Cycle.

For QOR the next interface state following address is a Quad Latency Cycle if there are latency cycles needed or Quad Output Cycle if no latency is required.

3.3.15 Quad Input Cycle - Host to Memory Transfer

The Quad I/O Read command transfers four address or mode bits to the memory in each cycle. The Quad Page Program command transfers four data bits to the memory in each cycle. The host keeps RESET# HIGH, CS# LOW, and drives the IO signals.

For Quad I/O Read the next interface state following the delivery of address and mode bits is a Quad Latency Cycle if there are latency cycles needed or Quad Output Cycle if no latency is required. For Quad Page Program the host returns CS# HIGH following the delivery of data to be programmed and the interface returns to standby state.

3.3.16 Quad Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR[7:6]). During the latency cycles, the host keeps RESET# HIGH, CS# LOW. The host may drive the IO signals during these cycles or the host may leave the IO floating. The memory does not use any data driven on IO during the latency cycles. The host must stop driving the IO signals on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the IO signals during the latency cycles.

The next interface state following the last latency cycle is a Quad Output Cycle.

3.3.17 Quad Output Cycle - Memory to Host Transfer

The Quad Output Read and Quad I/O Read return data to the host four bits in each cycle. The host keeps RESET# HIGH, and CS# LOW. The memory drives data on IO0-IO3 signals during the Quad output cycles.

The next interface state continues to be Quad Output Cycle until the host returns CS# to HIGH ending the command.

3.3.18 DDR Single Input Cycle - Host to Memory Transfer

The DDR Fast Read command sends address, and mode bits to the memory only on the IO0 signal. One bit is transferred on the rising edge of SCK and one bit on the falling edge in each cycle. The host keeps RESET# HIGH, and CS# LOW. The other IO signals are ignored by the memory.

The next interface state following the delivery of address and mode bits is a DDR Latency Cycle.

3.3.19 DDR Dual Input Cycle - Host to Memory Transfer

The DDR Dual I/O Read command sends address, and mode bits to the memory only on the IO0 and IO1 signals. Two bits are transferred on the rising edge of SCK and two bits on the falling edge in each cycle. The host keeps RESET# HIGH, and CS# LOW. The IO2 and IO3 signals are ignored by the memory.

The next interface state following the delivery of address and mode bits is a DDR Latency Cycle.

3.3.20 DDR Quad Input Cycle - Host to Memory Transfer

The DDR Quad I/O Read command sends address, and mode bits to the memory on all the IO signals. Four bits are transferred on the rising edge of SCK and four bits on the falling edge in each cycle. The host keeps RESET# HIGH, and CS# LOW.

The next interface state following the delivery of address and mode bits is a DDR Latency Cycle.

3.3.21 DDR Latency Cycle

DDR Read commands may have one to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR[7:6]). During the latency cycles, the host keeps RESET# HIGH and CS# LOW. The host may not drive the IO signals during these cycles. So that there is sufficient time for the host drivers to turn off before the memory begins to drive. This prevents driver conflict between host and memory when the signal direction changes. The memory has an option to drive all the IO signals with a Data Learning Pattern (DLP) during the last 4 latency cycles. The DLP option should not be enabled when there are fewer than five latency cycles so that there is at least one cycle of high impedance for turn around of the IO signals before the memory begins driving the DLP. When there are more than 4 cycles of latency the memory does not drive the IO signals until the last four cycles of latency.

The next interface state following the last latency cycle is a DDR Single, Dual, or Quad Output Cycle, depending on the instruction.

3.3.22 DDR Single Output Cycle - Memory to Host Transfer

The DDR Fast Read command returns bits to the host only on the SO / IO1 signal. One bit is transferred on the rising edge of SCK and one bit on the falling edge in each cycle. The host keeps RESET# HIGH, and CS# LOW. The other IO signals are not driven by the memory.

The next interface state continues to be DDR Single Output Cycle until the host returns CS# to HIGH ending the command.

3.3.23 DDR Dual Output Cycle - Memory to Host Transfer

The DDR Dual I/O Read command returns bits to the host only on the IO0 and IO1 signals. Two bits are transferred on the rising edge of SCK and two bits on the falling edge in each cycle. The host keeps RESET# HIGH, and CS# LOW. The IO2 and IO3 signals are not driven by the memory.

The next interface state continues to be DDR Dual Output Cycle until the host returns CS# to HIGH ending the command.

3.3.24 DDR Quad Output Cycle - Memory to Host Transfer

The DDR Quad I/O Read command returns bits to the host on all the IO signals. Four bits are transferred on the rising edge of SCK and four bits on the falling edge in each cycle. The host keeps RESET# HIGH, and CS# LOW.

The next interface state continues to be DDR Quad Output Cycle until the host returns CS# to HIGH ending the command.

3.4 Configuration Register Effects on the Interface

The configuration register bits 7 and 6 (CR1[7:6]) select the latency code for all read commands. The latency code selects the number of mode bit and latency cycles for each type of instruction.

The configuration register bit 1 (CR1[1]) selects whether Quad mode is enabled to ignore HOLD# and WP# and allow Quad Page Program, Quad Output Read, and Quad I/O Read commands. Quad mode must also be selected to allow Read DDR Quad I/O commands.

3.5 Data Protection

Some basic protection against unintended changes to stored data are provided and controlled purely by the hardware design. These are described below. Other software managed protection methods are discussed in the Software Interface on page 45 section of this document.

3.5.1 Power-Up

When the core supply voltage is at or below the V_{CC} (low) voltage, the device is considered to be powered off. The device does not react to external signals, and is prevented from performing any program or erase operation. Program and erase operations continue to be prevented during the Power-on Reset (POR) because no command is accepted until the exit from POR to the Interface Standby state.

3.5.2 Low Power

When V_{CC} is less than V_{CC} (cut-off) the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

3.5.3 Clock Pulse Count

The device verifies that all program, erase, and Write Registers (WRR) commands consist of a clock pulse count that is a multiple of eight before executing them. A command not having a multiple of 8 clock pulse count is ignored and no error status is set for the command.

4. Electrical Specifications

4.1 Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Storage Temperature Plastic Packages	–65°C to +150°C
Ambient Temperature with Power Applied	–65°C to +125°C
V_{CC}	–0.5V to +4.0V
V_{IO}[6]	–0.5V to +4.0V
Input voltage with respect to Ground (V_{SS})[7]	–0.5V to +(V_{IO} + 0.5V)
Output Short Circuit Current[8]	100 mA

Notes

6. V_{IO} must always be less than or equal V_{CC} + 200 mV.
7. See Section 4.3.3 Input Signal Overshoot on page 24 for allowed maximums during signal transition.
8. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
9. Stresses above those listed under Section 4 Absolute Maximum Ratings on page 23 may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 Thermal Resistance

Parameter	Description	Device	WNG008	SO316	FAB024	FAC024	Unit
Theta JA	Thermal resistance (junction to ambient)	S25FL128S	28	38	36	36	°C/W
		S25FL256	27	37	38	38	°C/W

4.3 Operating Ranges

Operating ranges define those limits between which the functionality of the device is guaranteed.

4.3.1 Power Supply Voltages

Some package options provide access to a separate input and output buffer power supply called V_{IO}. Packages which do not provide the separate V_{IO} connection, internally connect the device V_{IO} to V_{CC}. For these packages, the references to V_{IO} are also references to V_{CC}.

V_{CC}	2.7V to 3.6V
V_{IO}	1.65V to V_{CC} +200 mV

4.3.2 Temperature Ranges

Parameter	Symbol	Device	Spec		Unit
			Min	Max	
Ambient Temperature	T_A	Industrial (I)	–40	+85	°C
		Industrial Plus (V)	–40	+105	
		Extended (N)	–40	+125	
		Automotive, AEC-Q100 Grade 3 (A)	–40	+85	
		Automotive, AEC-Q100 Grade 2 (B)	–40	+105	
		Automotive AEC-Q100 Grade 1 (M)	–40	+125	

Note

10. Industrial Plus operating and performance parameters will be determined by device characterization and may vary from standard industrial temperature range devices as currently shown in this specification.

4.3.3 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{IO}. During voltage transitions, inputs or I/Os may overshoot V_{SS} to –2.0V or overshoot to V_{IO} +2.0V, for periods up to 20 ns.

Figure 19. Maximum Negative Overshoot Waveform

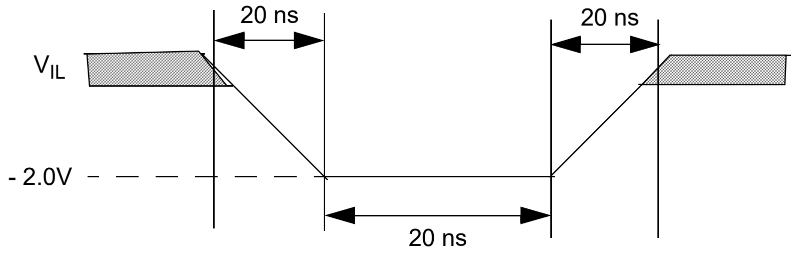
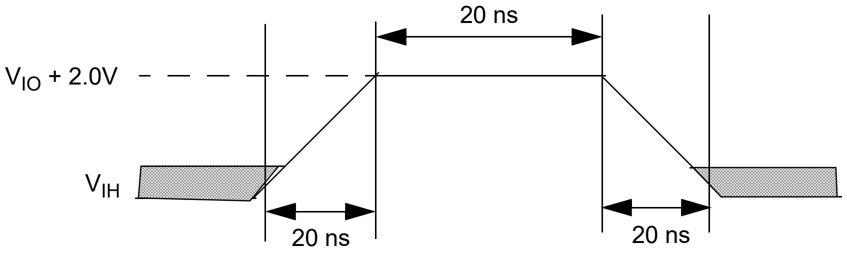


Figure 20. Maximum Positive Overshoot Waveform



4.4 Power-Up and Power-Down

The device must not be selected at power-up or power-down (that is, CS# must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value as follows:

- V_{CC} (min) at power-up, and then for a further delay of t_{PU}
- V_{SS} at power-down

A simple pull-up resistor (generally of the order of 100 kΩ) on Chip Select (CS#) can usually be used to insure safe and proper power-up and power-down.

The device ignores all instructions until a time delay of t_{PU} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold. See Figure 21. However, correct operation of the device is not guaranteed if V_{CC} returns below V_{CC} (min) during t_{PU}. No command should be sent to the device until the end of t_{PU}.

After power-up (t_{PU}), the device is in Standby mode (not Deep Power Down mode), draws CMOS standby current (I_{SB}), and the WEL bit is reset.

During power-down or voltage drops below V_{CC} (cut-off), the voltage must drop below V_{CC} (low) for a period of t_{PD} for the part to initialize correctly on power-up. See Figure 22. If during a voltage drop the V_{CC} stays above V_{CC} (cut-off) the part will stay initialized and will work correctly when V_{CC} is again above V_{CC} (min). In the event Power-on Reset (POR) did not complete correctly after power up, the assertion of the RESET# signal or receiving a software reset command (RESET) will restart the POR process.

Normal precautions must be taken for supply rail decoupling to stabilize the V_{CC} supply at the device. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package supply connection (this capacitor is generally of the order of 0.1 µf).

Table 5. Power-Up / Power-Down Voltage and Timing

Symbol	Parameter	Min	Max	Unit
V_{CC} (min)	V_{CC} (Minimum Operation Voltage)	2.7	–	V
V_{CC} (cut-off)	V_{CC} (Cut 0ff Where Re-initialization is Needed)	2.4	–	V
V_{CC} (low)	V_{CC} (Low Voltage for Initialization to Occur) V_{CC} (Low Voltage for Initialization to Occur at Embedded)	1.6 2.3	–	V
t_{PU}	V_{CC} (min) to Read Operation	–	300	µs
t_{PD}	V_{CC} (low) Time	15.0	–	µs

Figure 21. Power-Up

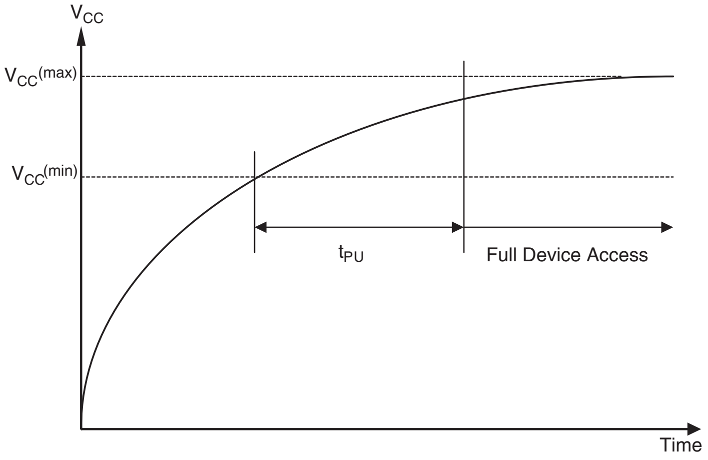
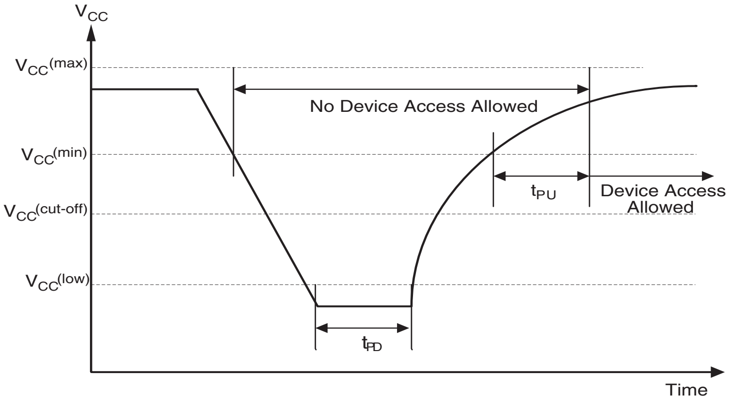


Figure 22. Power-Down and Voltage Drop



4.5 DC Characteristics

Applicable within operating ranges.

Table 6. DC Characteristics — Operating Temperature Range –40°C to +85°C

Symbol	Parameter	Test Conditions	Min	Typ[11]	Max	Unit
V_{IL}	Input Low Voltage		–0.5	–	0.2 x V_{IO}	V
V_{IH}	Input High Voltage		0.7 × V_{IO}	–	V_{IO}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA, V_{CC} = V_{CC} min	–	–	0.15 × V_{IO}	V
V_{OH}	Output High Voltage	I_{OH} = –0.1 mA	0.85 × V_{IO}	–		V
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{IH} or V_{IL}	–	–	±2	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{IH} or V_{IL}	–	–	±2	µA
I_{CC1}	Active Power Supply Current (READ)	Serial SDR@50 MHz Serial SDR@133 MHz Quad SDR@80 MHz Quad SDR@104 MHz Quad DDR@66 MHz Quad DDR@80 MHz Outputs unconnected during read data return[12]	–	–	16 33 50 61 75 90	mA
I_{CC2}	Active Power Supply Current (Page Program)	CS# = V_{IO}	–	–	100	mA
I_{CC3}	Active Power Supply Current (WRR)	CS# = V_{IO}	–	–	100	mA
I_{CC4}	Active Power Supply Current (SE)	CS# = V_{IO}	–	–	100	mA
I_{CC5}	Active Power Supply Current (BE)	CS# = V_{IO}	–	–	100	mA
I_{SB} (Industrial)	Standby Current	RESET#, CS# = V_{IO}; SI, SCK = V_{IO} or V_{SS}, Industrial Temp	–	70	100	µA
I_{SB} (Industrial Plus)	Standby Current	RESET#, CS# = V_{IO}; SI, SCK = V_{IO} or V_{SS}, Industrial Plus Temp	–	70	300	µA

Notes

[11] Typical values are at T_{AI} = 25°C and V_{CC} = V_{IO} = 3V.

[12] Output switching current is not included.

Table 7. DC Characteristics — Operating Temperature Range -40°C to +105°C and -40°C to +125°C

Symbol	Parameter	Test Conditions	Min	Typ[13]	Max	Unit
V_{IL}	Input Low Voltage		–0.5	–	0.2 x V_{IO}	V
V_{IH}	Input High Voltage		0.7 × V_{IO}	–	V_{IO}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA, V_{CC} = V_{CC} min		–	0.15 x V_{IO}	V
V_{OH}	Output High Voltage	I_{OH} = –0.1 mA	0.85 × V_{IO}	–		V
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{IH} or V_{IL}	–	–	±2	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{IH} or V_{IL}	–	–	±2	µA
I_{CC1}	Active Power Supply Current (READ)	Serial SDR@50 MHz Serial SDR@133 MHz Quad SDR@80 MHz Quad SDR@104 MHz Quad DDR@66 MHz Quad DDR@80 MHz Outputs unconnected during read data return[14]	–	–	22 35 50 61 75 90	mA
I_{CC2}	Active Power Supply Current (Page Program)	CS# = V_{IO}	–	–	100	mA
I_{CC3}	Active Power Supply Current (WRR)	CS# = V_{IO}	–	–	100	mA
I_{CC4}	Active Power Supply Current (SE)	CS# = V_{IO}	–	–	100	mA
I_{CC5}	Active Power Supply Current (BE)	CS# = V_{IO}	–	–	100	mA
I_{SB} (Industrial)	Standby Current	RESET#, CS# = V_{IO}; SI, SCK = V_{IO} or V_{SS}, Industrial Temp	–	70	100	µA
I_{SB} (Industrial Plus)	Standby Current	RESET#, CS# = V_{IO}; SI, SCK = V_{IO} or V_{SS}, Industrial Plus Temp	–	70	300	µA

Notes

13. Typical values are at T_{AI} = 25°C and V_{CC} = V_{IO} = 3V.
14. Output switching current is not included.

4.5.1 Active Power and Standby Power Modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is LOW. When CS# is HIGH, the device is disabled, but may still be in an Active Power mode until all program, erase, and write operations have completed. The device then goes into the Standby Power mode, and power consumption drops to I_{SB}.

5. Timing Specifications

5.1 Key to Switching Waveforms

Figure 23. Waveform Element Meanings

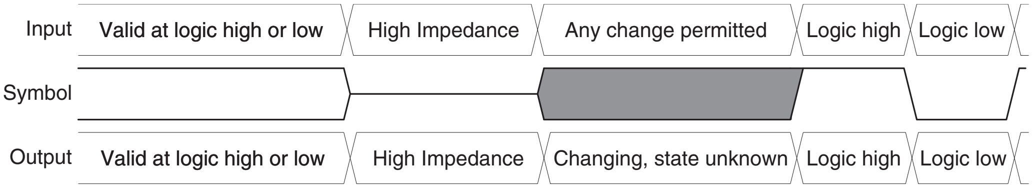
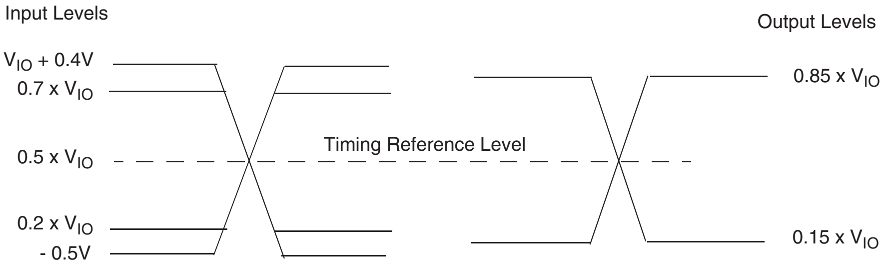


Figure 24. Input, Output, and Timing Reference Levels



5.2 AC Test Conditions

Figure 25. Test Setup

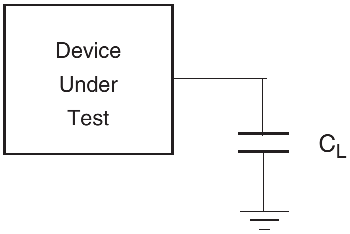


Table 8. AC Measurement Conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	30 15[18]		pF
	Input Rise and Fall Times	–	2.4	ns
	Input Pulse Voltage	0.2 x V_{IO} to 0.8 V_{IO}		V
	Input Timing Ref Voltage	0.5 V_{IO}		V
	Output Timing Ref Voltage	0.5 V_{IO}		V

Notes

15. Output High-Z is defined as the point where data is no longer driven.
16. Input slew rate: 1.5 V/ns.
17. AC characteristics tables assume clock and data signals have the same slew rate (slope).
18. DDR Operation.

5.2.1 Capacitance Characteristics

Table 9. Capacitance

	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance (applies to SCK, CS#, RESET#)	1 MHz	–	8	pF
C_{OUT}	Output Capacitance (applies to All I/O)	1 MHz	–	8	pF

Note

19. For more information on capacitance, please consult the IBIS models.

5.3 Reset

5.3.1 Power-On (Cold) Reset

The device executes a Power-On Reset (POR) process until a time delay of t_{PU} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold. See Figure 21 on page 25, Table 5 on page 25, and Table 10 on page 30. The device must not be selected (CS# to go HIGH with V_{IO}) during power-up (t_{PU}), i.e. no commands may be sent to the device until the end of t_{PU}. RESET# is ignored during POR. If RESET# is LOW during POR and remains low through and beyond the end of t_{PU}, CS# must remain HIGH until t_{RH} after RESET# returns HIGH. RESET# must return HIGH for greater than t_{RS} before returning low to initiate a hardware reset.

Figure 26. Reset LOW at the End of POR

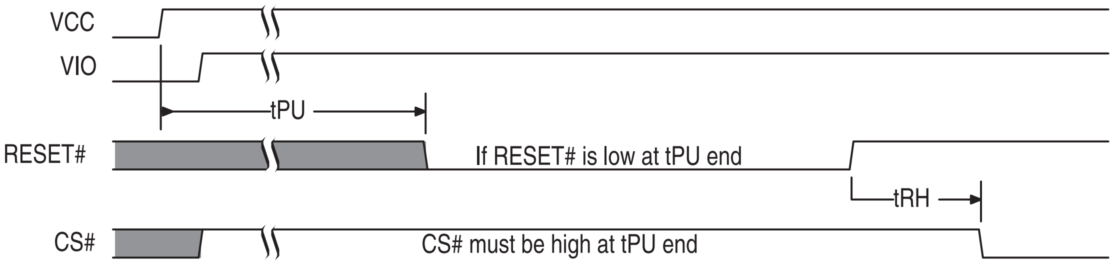


Figure 27. Reset HIGH at the End of POR

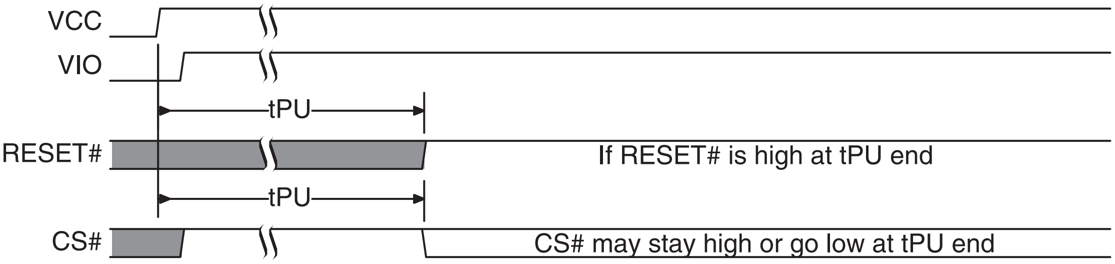
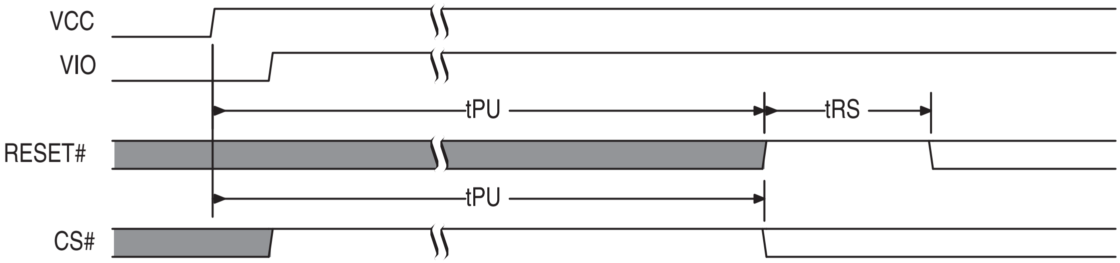


Figure 28. POR followed by Hardware Reset



5.3.2 Hardware (Warm) Reset

When the RESET# input transitions from V_{IH} to V_{IL} the device will reset register states in the same manner as power-on reset but, does not go through the full reset process that is performed during POR. The hardware reset process requires a period of t_{RPH} to complete. If the POR process did not complete correctly for any reason during power-up (t_{PU}), RESET# going LOW will initiate the full POR process instead of the hardware reset process and will require t_{PU} to complete the POR process.

The RESET# input provides a hardware method of resetting the flash memory device to standby state.

- RESET# must be HIGH for t_{RS} following t_{PU} or t_{RPH}, before going low again to initiate a hardware reset.
- When RESET# is driven low for at least a minimum period of time (t_{RP}), the device terminates any operation in progress, tri-states all outputs, and ignores all read/write commands for the duration of t_{RPH}. The device resets the interface to standby state.
- If CS# is LOW at the time RESET# is asserted, CS# must return HIGH during t_{RPH} before it can be asserted low again after t_{RH}.
- Hardware Reset is only offered in 16-lead SOIC and BGA packages.

Figure 29. Hardware Reset

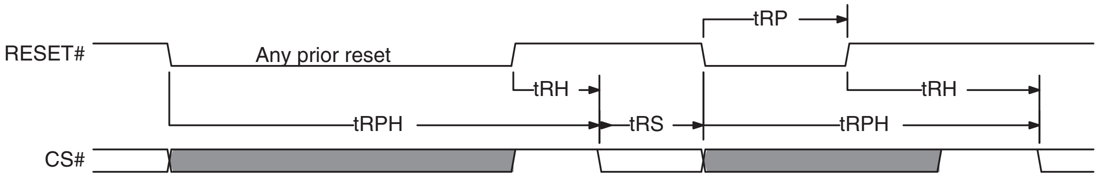


Table 10. Hardware Reset Parameters[20, 21]

Parameter	Description	Limit	Time	Unit
t_{RS}	Reset Setup - Prior Reset end and RESET# HIGH before RESET# LOW	Min	50	ns
t_{RPH}	Reset Pulse Hold - RESET# LOW to CS# LOW	Min	35	µs
t_{RP}	RESET# Pulse Width	Min	200	ns
t_{RH}	Reset Hold - RESET# HIGH before CS# LOW	Min	50	ns

Notes

20. RESET# LOW is optional and ignored during Power-up (t_{PU}). If Reset# is asserted during the end of t_{PU}, the device will remain in the reset state and t_{RH} will determine when CS# may go LOW.
21. Sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.

5.4 SDR AC Characteristics

Table 11. AC Characteristics (Single Die Package, V_{IO} = V_{CC} 2.7V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
$F_{SCK, R}$	SCK Clock Frequency for READ and 4READ instructions	DC	–	50	MHz
$F_{SCK, C}$	SCK Clock Frequency for single commands as shown in Table 44 on page 66[25]	DC	–	133	MHz
$F_{SCK, C}$	SCK Clock Frequency for the following dual and quad commands: DOR, 4DOR, QOR, 4QOR, DIOR, 4DIOR, QIOR, 4QIOR	DC	–	104	MHz
$F_{SCK, QPP}$	SCK Clock Frequency for the QPP, 4QPP commands	DC	–	80	MHz
P_{SCK}	SCK Clock Period	1/ F_{SCK}	–	∞	
t_{WH}, t_{CH}	Clock High Time[26]	45% P_{SCK}	–	–	ns
t_{WL}, t_{CL}	Clock Low Time[26]	45% P_{SCK}	–	–	ns
t_{CRT}, t_{CLCH}	Clock Rise Time (slew rate)	0.1	–	–	V/ns
t_{CFT}, t_{CHCL}	Clock Fall Time (slew rate)	0.1	–	–	V/ns
t_{CS}	CS# High Time (Read Instructions) CS# High Time (Program/Erase)	10 50	–	–	ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3	–	–	ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	3	–	–	ns
t_{SU}	Data in Setup Time	1.5	–	3000[27]	ns
t_{HD}	Data in Hold Time	2	–	–	ns
t_{V}	Clock Low to Output Valid	–	–	8.0[23] 7.65[24] 6.5[25]	ns
t_{HO}	Output Hold Time	2	–		ns
t_{DIS}	Output Disable Time	0	–	8	ns
t_{WPS}	WP# Setup Time	20[22]	–	–	ns
t_{WPH}	WP# Hold Time	100[22]	–	–	ns
t_{HLCH}	HOLD# Active Setup Time (relative to SCK)	3	–	–	ns
t_{CHHH}	HOLD# Active Hold Time (relative to SCK)	3	–	–	ns
t_{HHCH}	HOLD# Non Active Setup Time (relative to SCK)	3	–	–	ns
t_{CHHL}	HOLD# Non Active Hold Time (relative to SCK)	3	–	–	ns
t_{HZ}	HOLD# enable to Output Invalid	–	–	8	ns
t_{LZ}	HOLD# disable to Output Valid	–	–	8	ns

Notes

22. Only applicable as a constraint for WRR instruction when SRWD is set to a 1.
23. Full V_{CC} range (2.7 - 3.6V) and CL = 30 pF.
24. Regulated V_{CC} range (3.0 - 3.6V) and CL = 30 pF.
25. Regulated V_{CC} range (3.0 - 3.6V) and CL = 15 pF.
26. ±10% duty cycle is supported for frequencies $\leq$ 50 MHz.
27. Maximum value only applies during Program/Erase Suspend/Resume commands.

Table 12. AC Characteristics (Single Die Package, V_{IO} 1.65V to 2.7V, V_{CC} 2.7V to 3.6V)

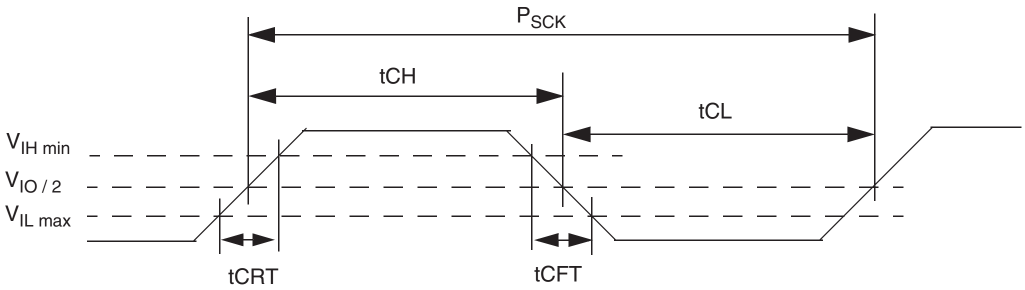
Symbol	Parameter	Min	Typ	Max	Unit
$F_{SCK, R}$	SCK Clock Frequency for READ, 4READ instructions	DC	–	50	MHz
$F_{SCK, C}$	SCK Clock Frequency for all others[30]	DC	–	66	MHz
P_{SCK}	SCK Clock Period	1/ F_{SCK}	–	∞	
t_{WH}, t_{CH}	Clock High Time[31]	45% P_{SCK}	–	–	ns
t_{WL}, t_{CL}	Clock Low Time[31]	45% P_{SCK}	–	–	ns
t_{CRT}, t_{CLCH}	Clock Rise Time (slew rate)	0.1	–	–	V/ns
t_{CFT}, t_{CHCL}	Clock Fall Time (slew rate)	0.1	–	–	V/ns
t_{CS}	CS# High Time (Read Instructions) CS# High Time (Program/Erase)	10 50	–	–	ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	10	–	–	ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	3	–	–	ns
t_{SU}	Data in Setup Time	5	–	3000[32]	ns
t_{HD}	Data in Hold Time	4	–	–	ns
t_V	Clock Low to Output Valid	–	–	14.5[29] 12.0[30]	ns
t_{HO}	Output Hold Time	2	–		ns
t_{DIS}	Output Disable Time	0	–	14	ns
t_{WPS}	WP# Setup Time	20[28]	–	–	ns
t_{WPH}	WP# Hold Time	100[28]	–	–	ns
t_{HLCH}	HOLD# Active Setup Time (relative to SCK)	5	–	–	ns
t_{CHHH}	HOLD# Active Hold Time (relative to SCK)	5	–	–	ns
t_{HHCH}	HOLD# Non Active Setup Time (relative to SCK)	5	–	–	ns
t_{CHHL}	HOLD# Non Active Hold Time (relative to SCK)	5	–	–	ns
t_{HZ}	HOLD# enable to Output Invalid	–	–	14	ns
t_{LZ}	HOLD# disable to Output Valid	–	–	14	ns

Notes

28. Only applicable as a constraint for WRR instruction when SRWD is set to a 1.
29. CL = 30 pF.
30. CL = 15 pF.
31. ±10% duty cycle is supported for frequencies ≤ 50 MHz.
32. Maximum value only applies during Program/Erase Suspend/Resume commands.

5.4.1 Clock Timing

Figure 30. Clock Timing



5.4.2 Input / Output Timing

Figure 31. SPI Single Bit Input Timing

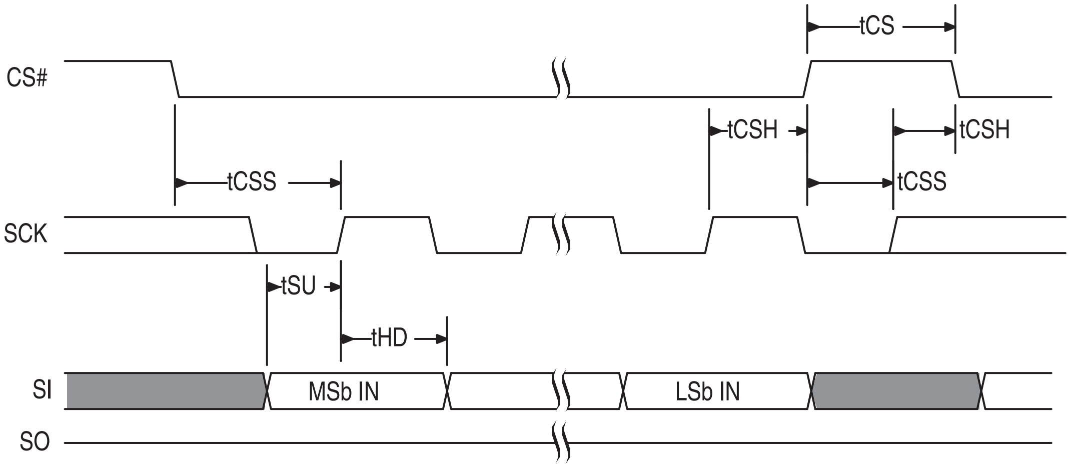


Figure 32. SPI Single Bit Output Timing

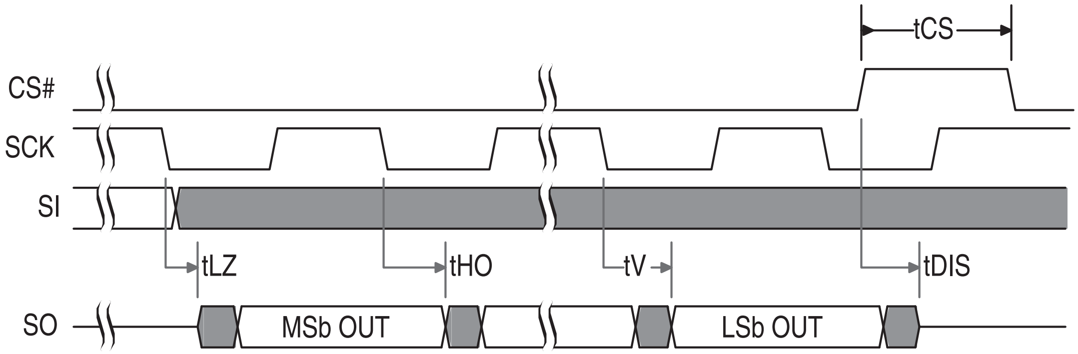


Figure 33. SPI SDR MIO Timing

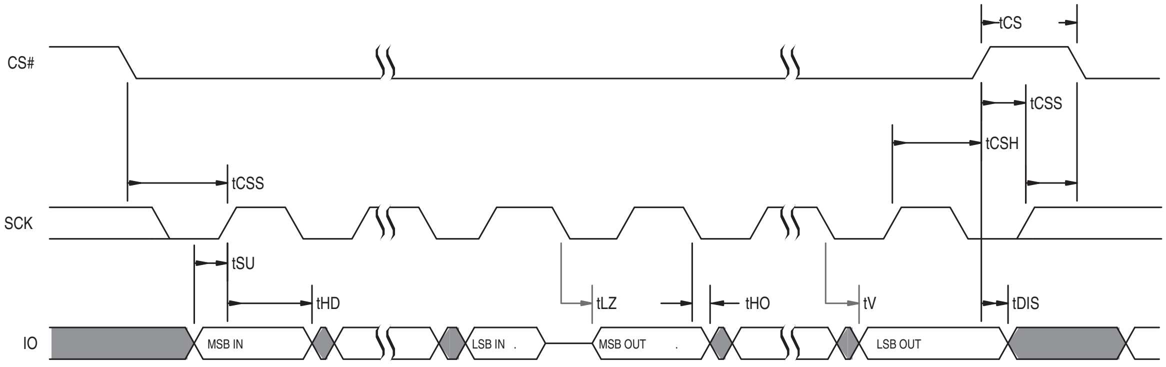


Figure 34. Hold Timing

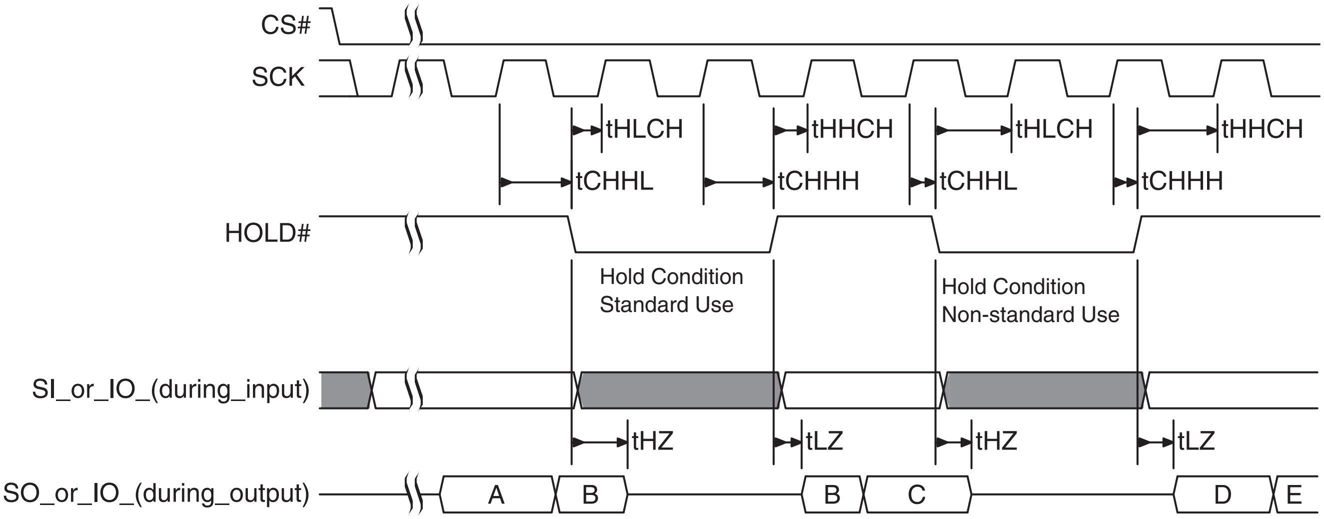
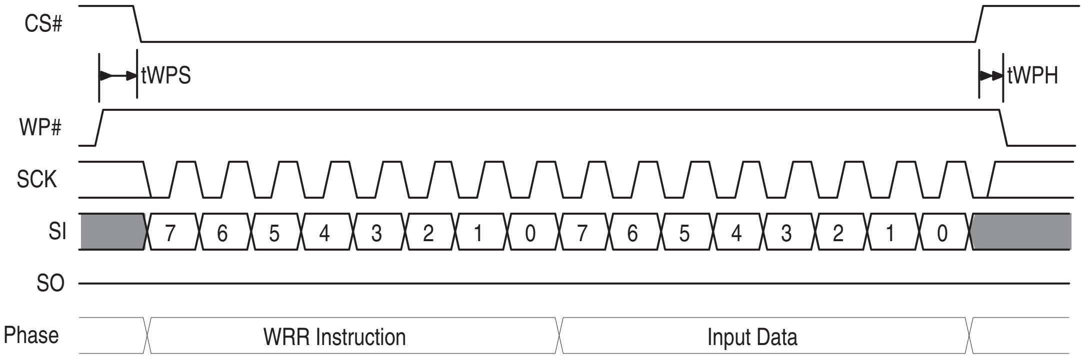


Figure 35. WP# Input Timing



5.5 DDR AC Characteristics

Table 13. AC Characteristics — DDR Operation

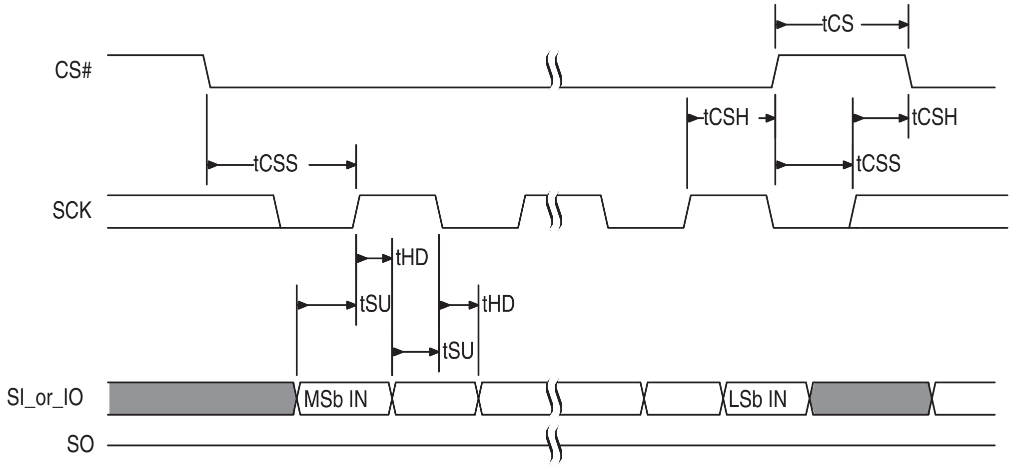
Symbol	Parameter	66 MHz			80 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
$F_{SCK, R}$	SCK Clock Frequency for DDR READ instruction	DC	–	66	DC	–	80	MHz
$P_{SCK, R}$	SCK Clock Period for DDR READ instruction	15	–	∞	12.5	–	∞	ns
t_{WH}, t_{CH}	Clock High Time	45% P_{SCK}	–	–	45% P_{SCK}	–	–	ns
t_{WL}, t_{CL}	Clock Low Time	45% P_{SCK}	–	–	45% P_{SCK}	–	–	ns
t_{CS}	CS# High Time (Read Instructions)	10	–	–	10	–	–	ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3	–	–	3	–	–	ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	3	–	–	3	–	–	ns
t_{SU}	IO in Setup Time	2	–	3000[34]	1.5	–	3000[34]	ns
t_{HD}	IO in Hold Time	2	–	–	1.5	–	–	ns
t_V	Clock Low to Output Valid	–	–	6.5[33]	–	–	6.5[33]	ns
t_{HO}	Output Hold Time	1.5	–		1.5	–	–	ns
t_{DIS}	Output Disable Time	–	–	8	–	–	8	ns
t_{LZ}	Clock to Output Low Impedance	0	–	8	0	–	8	ns
t_{O_SKEW}	First Output to last Output data valid time	–	–	600	–	–	600	ps

Notes

33. Regulated V_{CC} range (3.0 - 3.6V) and CL = 15 pF.
34. Maximum value only applies during Program/Erase Suspend/Resume commands.

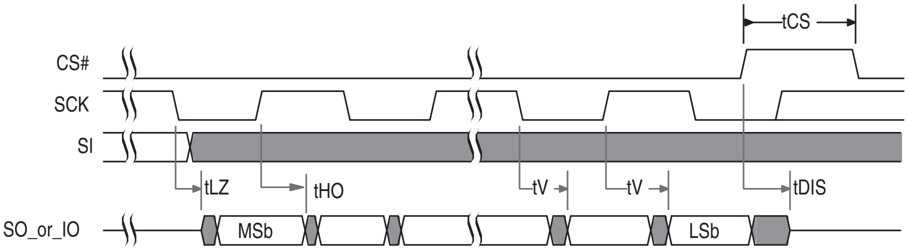
5.5.1 DDR Input Timing

Figure 36. SPI DDR Input Timing



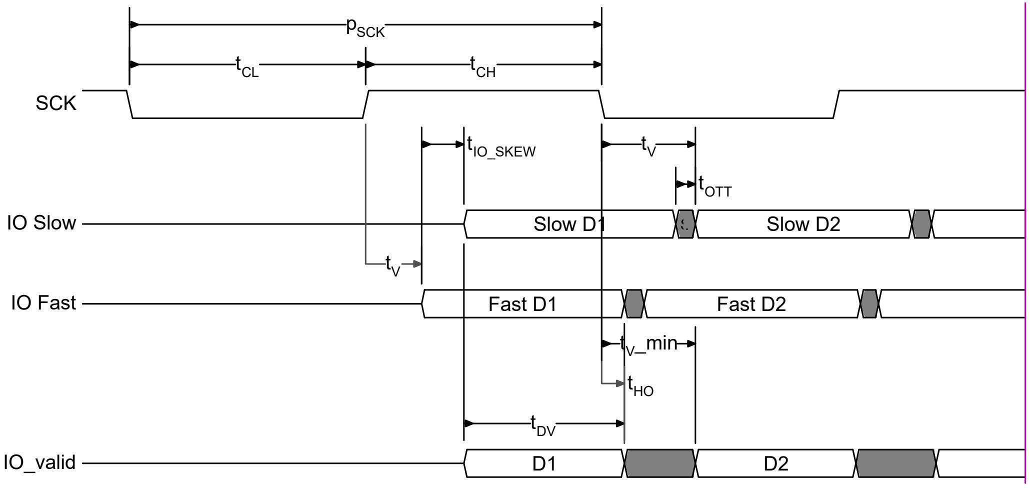
5.5.2 DDR Output Timing

Figure 37. SPI DDR Output Timing



5.5.3 DDR Data Valid Timing Using DLP

Figure 38. SPI DDR Data Valid Window



The minimum data valid window (t_{DV}) and t_V minimum can be calculated as follows:

t_{DV} = Minimum half clock cycle time (t_{CLH})[35] - t_{OTT}[35] - t_{IO_SKEW}[36]

t_V _min = t_{HO} + t_{IO_SKEW} + t_{OTT}

Example:

80 MHz clock frequency = 12.5 ns clock period, DDR operations and duty cycle of 45% or higher

t_{CLH} = 0.45 x PSCK = 0.45 x 12.5 ns = 5.625 ns

Bus impedance of 45 ohm and capacitance of 22 pf, with timing reference of $0.75V_{CC}$, the rise time from 0 to 1 or fall time 1 to 0 is 1.4[40] x RC time constant (Tau)[39] = 1.4 x 0.99 ns = 1.39 ns

t_{OTT} = rise time or fall time = 1.39 ns.

Data Valid Window

t_{DV} = t_{CLH} - t_{IO_SKEW} - t_{OTT} = 5.625 ns - 600 ps - 1.39 ns = 3.635 ns

t_V Minimum

t_V _min = t_{HO} + t_{IO_SKEW} + t_{OTT} = 1.0 ns + 600 ps + 1.39 ns = 2.99 ns

Notes

35. t_{CLH} is the shorter duration of t_{CL} or t_{CH}.
36. t_{IO_SKEW} is the maximum difference (delta) between the minimum and maximum t_V (output valid) across all IO signals.
37. t_{OTT} is the maximum Output Transition Time from one valid data value to the next valid data value on each IO. t_{OTT} is dependent on system level considerations including:
    a. Memory device output impedance (drive strength).
    b. System level parasitics on the IOs (primarily bus capacitance).
    c. Host memory controller input V_{IH} and V_{IL} levels at which 0 to 1 and 1 to 0 transitions are recognized.
    d. t_{OTT} is not a specification tested by Cypress, it is system dependent and must be derived by the system designer based on the above considerations.
38. t_{DV} is the data valid window.
39. Tau = R (Output Impedance) x C (Load capacitance).
40. Multiplier of Tau time for voltage to rise to 75% of V_{CC}.

6. Physical Interface

Table 14. Model Specific Connections[41]

VIO / RFU	Versatile I/O or RFU — Some device models bond this connector to the device I/O power supply, other models bond the device I/O supply to Vcc within the package leaving this package connector unconnected.
RESET# / RFU	RESET# or RFU — Some device models bond this connector to the device RESET# signal, other models bond the RESET# signal to Vcc within the package leaving this package connector unconnected.

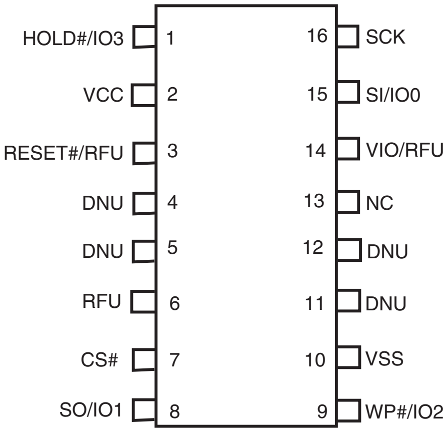
Note

41. Refer to Table 2 on page 8 for signal descriptions.

6.1 SOIC 16-Lead Package

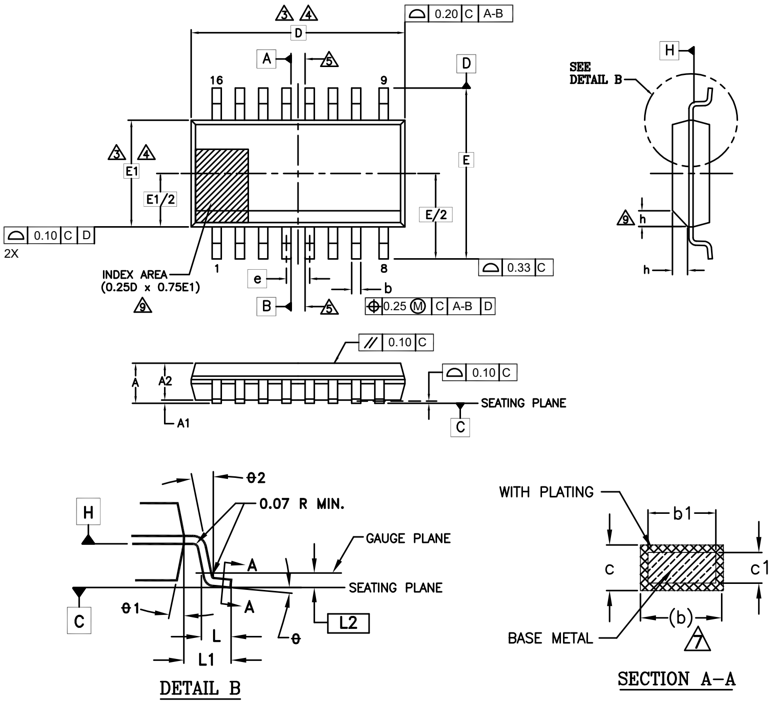
6.1.1 SOIC 16 Connection Diagram

Figure 39. 16-Lead SOIC Package, Top View



6.1.2 SOIC 16 Physical Diagram

Figure 40. S03016 — 16-Lead Wide Plastic Small Outline Package (300-mil Body Width)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.35	-	2.65
A1	0.10	-	0.30
A2	2.05	-	2.55
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.20	-	0.33
c1	0.20	-	0.30
D	10.30 BSC		
E	10.30 BSC		
E1	7.50 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.40 REF		
L2	0.25 BSC		
N	16		
h	0.25	-	0.75
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

NOTES:

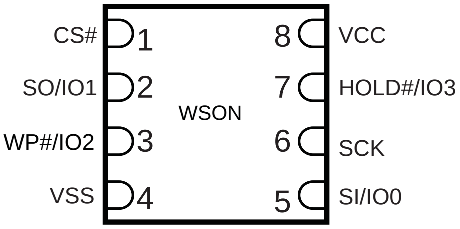
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

002-15547 *A

6.2 WSON Package

6.2.1 WSON Connection Diagram

Figure 41. Leadless Package (WSON), Top View[42]

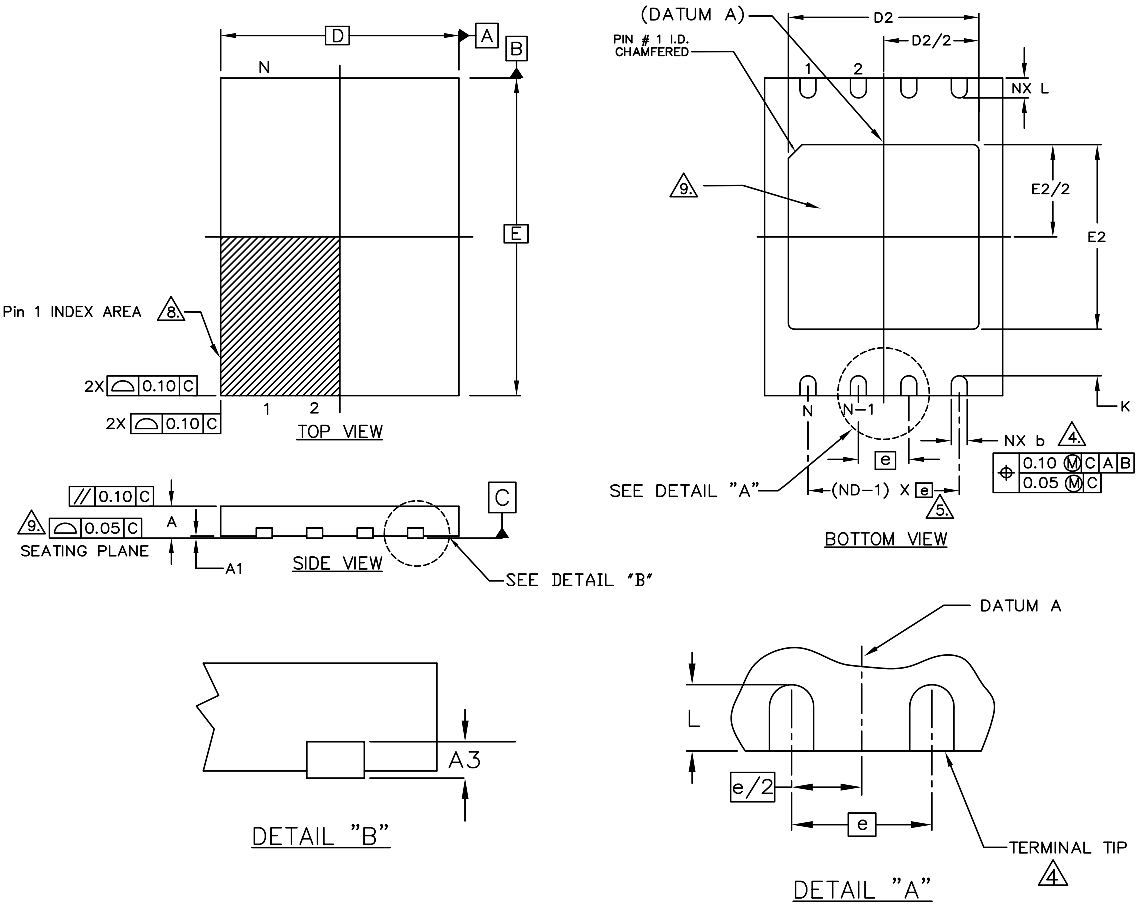


Note

42. RESET# and V_{IO} are pulled to V_{CC} internal to the memory device.

6.2.2 WSON Physical Diagram

Figure 42. WNG008 — WSON 8-Contact (6 x 8 mm) No-Lead Package



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e	1.27 BSC.		
N	8		
ND	4		
L	0.45	0.50	0.55
b	0.35	0.40	0.45
D2	4.70	4.80	4.90
E2	4.55	4.65	4.75
D	6.00 BSC		
E	8.00 BSC		
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
K	0.20 MIN.		

NOTES:

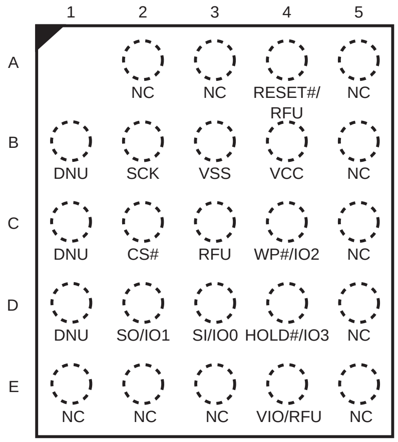
1. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. A MAXIMUM 0.15mm PULL BACK (L1) MAY BE PRESENT.

002-18827 **

6.3 FAB024 24-Ball BGA Package

6.3.1 Connection Diagram

Figure 43. 24-Ball BGA, 5 x 5 Ball Footprint (FAB024), Top View[43]

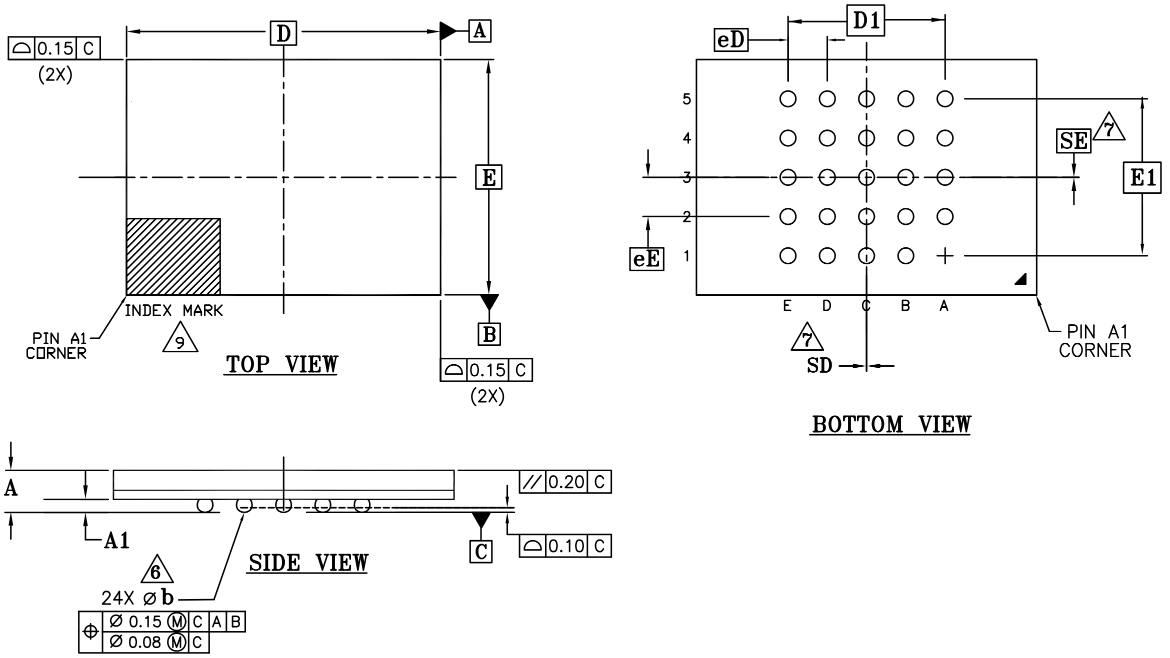


Note

[43] Signal connections are in the same relative positions as FAC024 BGA, allowing a single PCB footprint to use either package.

6.3.2 FAB024 24-Ball BGA Package Physical Diagram

Figure 44. FAB024 — 24-Ball BGA (8 x 6 mm) Package



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.20	-	-
D	8.00 BSC		
E	6.00 BSC		
D1	4.00 BSC		
E1	4.00 BSC		
MD	5		
ME	5		
N	24		
Ø b	0.35	0.40	0.45
eE	1.00 BSC		
eD	1.00 BSC		
SD	0.00 BSC		
SE	0.00 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7 "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.

WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

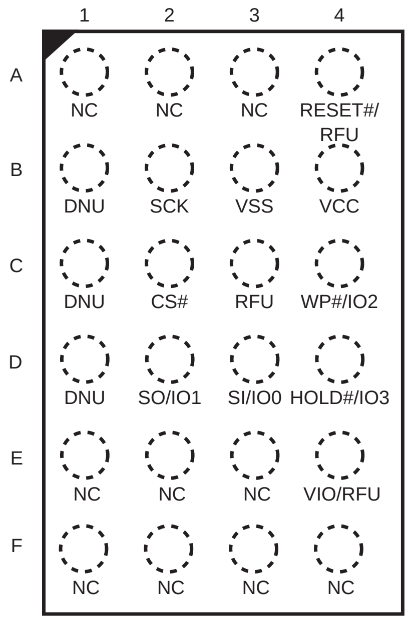
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

002-15534 **

6.4 FAC024 24-Ball BGA Package

6.4.1 Connection Diagram

Figure 45. 24-Ball BGA, 4 x 6 Ball Footprint (FAC024), Top View[44]



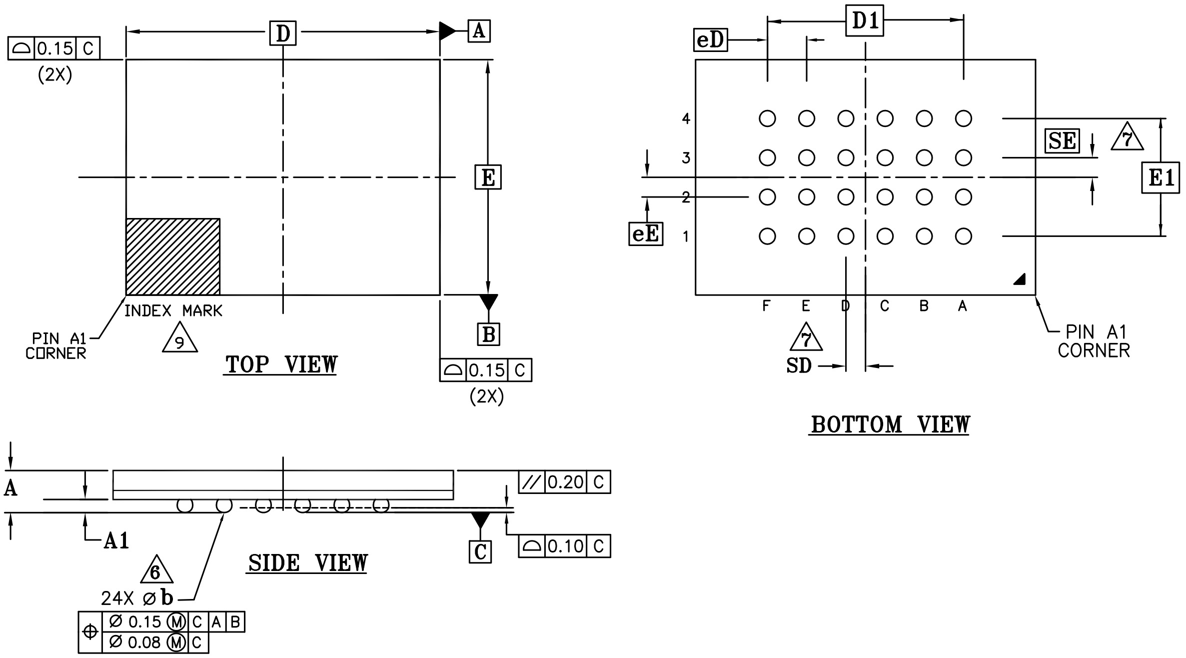
	1	2	3	4
A	NC	NC	NC	RESET#/ RFU
B	DNU	SCK	VSS	VCC
C	DNU	CS#	RFU	WP#/IO2
D	DNU	SO/IO1	SI/IO0	HOLD#/IO3
E	NC	NC	NC	VIO/RFU
F	NC	NC	NC	NC

Note

[44] Signal connections are in the same relative positions as FAB024 BGA, allowing a single PCB footprint to use either package.

6.4.2 FAC024 24-Ball BGA Package Physical Diagram

Figure 46. FAC024 — 24-Ball BGA (6 x 8 mm) Package



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.25	-	-
D	8.00 BSC		
E	6.00 BSC		
D1	5.00 BSC		
E1	3.00 BSC		
MD	6		
ME	4		
N	24		
⌀ b	0.35	0.40	0.45
eE	1.00 BSC		
eD	1.00 BSC		
SD	0.50 BSC		
SE	0.50 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. $\boxed{e}$ REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

002-15535 **

6.4.3 Special Handling Instructions for FBGA Packages

Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

Software Interface

This section discusses the features and behaviors most relevant to host system software that interacts with S25FL128S and S25FL256S memory devices.

7. Address Space Maps

7.1 Overview

7.1.1 Extended Address

The S25FL128S and S25FL256S devices support 32-bit addresses to enable higher density devices than allowed by previous generation (legacy) SPI devices that supported only 24-bit addresses. A 24-bit byte resolution address can access only 16 MB (128 Mb) of maximum density. A 32-bit byte resolution address allows direct addressing of up to a 4 Gbytes (32 Gbits) of address space.

Legacy commands continue to support 24-bit addresses for backward software compatibility. Extended 32-bit addresses are enabled in three ways:

- Bank address register — a software (command) loadable internal register that supplies the high order bits of address when legacy 24-bit addresses are in use.
- Extended address mode — a bank address register bit that changes all legacy commands to expect 32 bits of address supplied from the host system.
- New commands — that perform both legacy and new functions, which expect 32-bit address.

The default condition at power-up and after reset, is the Bank address register loaded with zeros and the extended address mode set for 24-bit addresses. This enables legacy software compatible access to the first 128 Mb of a device.

The S25FL128S device supports the extended address features in the same way but in essence ignores bits 31 to 24 of any address because the main flash array only needs 24 bits of address. This enables simple migration from the 128-Mb density to higher density devices without changing the address handling aspects of software.

7.1.2 Multiple Address Spaces

Many commands operate on the main flash memory array. Some commands operate on address spaces separate from the main flash array. Each separate address space uses the full 32-bit address but may only define a small portion of the available address space.

7.2 Flash Memory Array

The main flash array is divided into erase units called sectors. The sectors are organized either as a hybrid combination of 4-KB and 64-KB sectors, or as uniform 256-KB sectors. The sector organization depends on the device model selected, see Section 12. Ordering Information on page 140.

Table 15. S25FL256S Sector and Memory Address Map, Bottom 4-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
4	32	SA00	00000000h-00000FFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA31	0001F000h-0001FFFFh	
64	510	SA32	00020000h-0002FFFFh	
		:	:	
		SA541	01FF0000h-01FFFFFFh	

Table 16. S25FL256S Sector and Memory Address Map, Top 4-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
64	510	SA00	0000000h-000FFFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA509	01FD0000h-01FDFFFFh	
4	32	SA510	01FE0000h-01FE0FFFh	
		:	:	
		SA541	01FFF000h-01FFFFFFh	

Table 17. S25FL256S Sector and Memory Address Map, Uniform 256-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (8-bit)	Notes
256	128	SA00	0000000h-003FFFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA127	1FC0000h-1FFFFFFh	

Table 18. S25FL128S Sector and Memory Address Map, Bottom 4-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
4	32	SA00	00000000h-00000FFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA31	0001F000h-0001FFFFh	
64	254	SA32	00020000h-0002FFFFh	
		:	:	
		SA285	00FF0000h-00FFFFFFh	

Table 19. S25FL128S Sector and Memory Address Map, Top 4-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
64	254	SA00	0000000h-000FFFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA253	00FD0000h-00FDFFFFh	
4	32	SA254	00FE0000h-00FE0FFFh	
		:	:	
		SA285	00FFF000h-00FFFFFFh	

Table 20. S25FL128S Sector and Memory Address Map, Uniform 256-KB Sectors

Sector Size (KB)	Sector Count	Sector Range	Address Range (Byte Address)	Notes
256	64	SA00	0000000h-003FFFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA63	0FC0000h-0FFFFFFh	

Note: These are condensed tables that use a couple of sectors as references. There are address ranges that are not explicitly listed. All 256 KB sectors have the pattern XXX0000h-XXXFFFFh.

7.3 ID-CFI Address Space

The RDID command (9Fh) reads information from a separate flash memory address space for device identification (ID) and Common Flash Interface (CFI) information. See Section 11.2 Device ID and Common Flash Interface (ID-CFI) Address Map on page 123 for the tables defining the contents of the ID-CFI address space. The ID-CFI address space is programmed by Cypress and read-only for the host system.

7.4 OTP Address Space

Each S25FL128S and S25FL256S memory device has a 1024-byte One Time Program (OTP) address space that is separate from the main flash array. The OTP area is divided into 32, individually lockable, 32-byte aligned and length regions.

In the 32-byte region starting at address zero:

- The 16 lowest address bytes are programmed by Cypress with a 128-bit random number. Only Cypress is able to program these bytes.
- The next 4 higher address bytes (OTP Lock Bytes) are used to provide one bit per OTP region to permanently protect each
- region from programming. The bytes are erased when shipped from Cypress. After an OTP region is programmed, it can be locked to prevent further programming, by programming the related protection bit in the OTP Lock Bytes.
- The next higher 12 bytes of the lowest address region are Reserved for Future Use (RFU). The bits in these RFU bytes may be programmed by the host system but it must be understood that a future device may use those bits for protection of a larger OTP space. The bytes are erased when shipped from Cypress.

The remaining regions are erased when shipped from Cypress, and are available for programming of additional permanent data.

Refer to Figure 47 on page 48 for a pictorial representation of the OTP memory space.

The OTP memory space is intended for increased system security. OTP values, such as the random number programmed by Cypress, can be used to “mate” a flash component with the system CPU/ASIC to prevent device substitution.

The configuration register FREEZE (CR1[0]) bit protects the entire OTP memory space from programming when set to 1. This allows trusted boot code to control programming of OTP regions then set the FREEZE bit to prevent further OTP memory space programming during the remainder of normal power-on system operation.

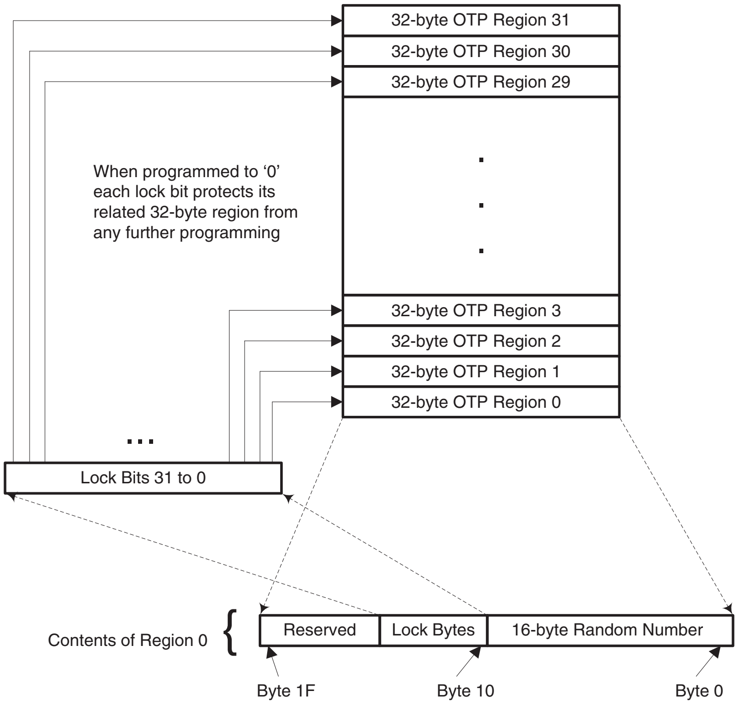


Figure 47. OTP Address Space

Table 21. OTP Address Map

Region	Byte Address Range (Hex)	Contents	Initial Delivery State (Hex)
Region 0	000	Least Significant Byte of Cypress Programmed Random Number	Cypress Programmed Random Number
	...	...	
	00F	Most Significant Byte of Cypress Programmed Random Number	
	010 to 013	Region Locking Bits Byte 10 [bit 0] locks region 0 from programming when = 0 ... Byte 13 [bit 7] locks region 31 from programming when = 0	All bytes = FF
	014 to 01F	Reserved for Future Use (RFU)	All bytes = FF
Region 1	020 to 03F	Available for User Programming	All bytes = FF
Region 2	040 to 05F	Available for User Programming	All bytes = FF
...	...	Available for User Programming	All bytes = FF
Region 31	3E0 to 3FF	Available for User Programming	All bytes = FF

7.5 Registers

Registers are small groups of memory cells used to configure how the S25FL-S memory device operates or to report the status of device operations. The registers are accessed by specific commands. The commands (and hexadecimal instruction codes) used for each register are noted in each register description. The individual register bits may be volatile, non-volatile, or One Time Programmable (OTP). The type for each bit is noted in each register description. The default state shown for each bit refers to the state after power-on reset, hardware reset, or software reset if the bit is volatile. If the bit is non-volatile or OTP, the default state is the value of the bit when the device is shipped from Cypress. Non-volatile bits have the same cycling (erase and program) endurance as the main flash array.

Table 22. Register Descriptions

Register	Abbreviation	Type	Bit Location
Status Register 1	SR1[7:0]	Volatile	7:0
Configuration Register 1	CR1[7:0]	Volatile	7:0
Status Register 2	SR2[7:0]	RFU	7:0
AutoBoot Register	ABRD[31:0]	Non-volatile	31:0
Bank Address Register	BRAC[7:0]	Volatile	7:0
ECC Status Register	ECCSR[7:0]	Volatile	7:0
ASP Register	ASPR[15:1]	OTP	15:1
ASP Register	ASPR[0]	RFU	0
Password Register	PASS[63:0]	Non-volatile OTP	63:0
PPB Lock Register	PPBL[7:1]	Volatile	7:1
PPB Lock Register	PPBL[0]	Volatile Read Only	0
PPB Access Register	PPBAR[7:0]	Non-volatile	7:0
DYB Access Register	DYBAR[7:0]	Volatile	7:0
SPI DDR Data Learning Registers	NVDLR[7:0]	Non-volatile	7:0
SPI DDR Data Learning Registers	VDLR[7:0]	Volatile	7:0

7.5.1 Status Register 1 (SR1)

Related Commands: Read Status Register (RDSR1 05h), Write Registers (WRR 01h), Write Enable (WREN 06h), Write Disable (WRDI 04h), Clear Status Register (CLSR 30h).

Table 23. Status Register 1 (SR1)

Bits	Field Name	Function	Type	Default State	Description
7	SRWD	Status Register Write Disable	Non-Volatile	0	1 = Locks state of SRWD, BP, and configuration register bits when WP# is LOW by ignoring WRR command 0 = No protection, even when WP# is LOW
6	P_ERR	Programming Error Occurred	Volatile, Read only	0	1 = Error occurred. 0 = No Error
5	E_ERR	Erase Error Occurred	Volatile, Read only	0	1 = Error occurred 0 = No Error
4	BP2	Block Protection	Volatile if CR1[3]=1, Non-Volatile if CR1[3]=0	1 if CR1[3]=1, 0 when shipped from Cypress	Protects selected range of sectors (Block) from Program or Erase
3	BP1				
2	BP0				
1	WEL	Write Enable Latch	Volatile	0	1 = Device accepts Write Registers (WRR), program or erase commands 0 = Device ignores Write Registers (WRR), program or erase commands This bit is not affected by WRR, only WREN and WRDI commands affect this bit
0	WIP	Write in Progress	Volatile, Read only	0	1 = Device Busy, a Write Registers (WRR), program, erase or other operation is in progress 0 = Ready Device is in standby mode and can accept commands

The Status Register contains both status and control bits:

Status Register Write Disable (SRWD) SR1[7]: Places the device in the Hardware Protected mode when this bit is set to 1 and the WP# input is driven low. In this mode, the SRWD, BP2, BP1, and BP0 bits of the Status Register become read-only bits and the Write Registers (WRR) command is no longer accepted for execution. If WP# is HIGH the SRWD bit and BP bits may be changed by the WRR command. If SRWD is 0, WP# has no effect and the SRWD bit and BP bits may be changed by the WRR command. The SRWD bit has the same non-volatile endurance as the main flash array.

Program Error (P_ERR) SR1[6]: The Program Error Bit is used as a program operation success or failure indication. When the Program Error bit is set to a 1 it indicates that there was an error in the last program operation. This bit will also be set when the user attempts to program within a protected main memory sector or locked OTP region. When the Program Error bit is set to a 1 this bit can be reset to 0 with the Clear Status Register (CLSR) command. This is a read-only bit and is not affected by the WRR command.

Erase Error (E_ERR) SR1[5]: The Erase Error Bit is used as an Erase operation success or failure indication. When the Erase Error bit is set to a 1 it indicates that there was an error in the last erase operation. This bit will also be set when the user attempts to erase an individual protected main memory sector. The Bulk Erase command will not set E_ERR if a protected sector is found during the command execution. When the Erase Error bit is set to a 1 this bit can be reset to 0 with the Clear Status Register (CLSR) command. This is a read-only bit and is not affected by the WRR command.

Block Protection (BP2, BP1, BP0) SR1[4:2]: These bits define the main flash array area to be software-protected against program and erase commands. The BP bits are either volatile or non-volatile, depending on the state of the BP non-volatile bit (BPNV) in the configuration register. When one or more of the BP bits is set to 1, the relevant memory area is protected against program and erase. The Bulk Erase (BE) command can be executed only when the BP bits are cleared to 0's. See Section 8.3 Block Protection on page 59 for a description of how the BP bit values select the memory array area protected. The BP bits have the same non-volatile endurance as the main flash array.

Write Enable Latch (WEL) SR1[1]: The WEL bit must be set to 1 to enable program, write, or erase operations as a means to provide protection against inadvertent changes to memory or register values. The Write Enable (WREN) command execution sets the Write Enable Latch to a 1 to allow any program, erase, or write commands to execute afterwards. The Write Disable (WRDI) command can be used to set the Write Enable Latch to a 0 to prevent all program, erase, and write commands from execution. The WEL bit is cleared to 0 at the end of any successful program, write, or erase operation. Following a failed operation, the WEL bit may remain set and should be cleared with a WRDI command following a CLSR command. After a power down/power up sequence, hardware reset, or software reset, the Write Enable Latch is set to a 0 The WRR command does not affect this bit.

Write In Progress (WIP) SR1[0]: Indicates whether the device is performing a program, write, erase operation, or any other operation, during which a new operation command will be ignored. When the bit is set to a 1 the device is busy performing an operation. While WIP is 1, only Read Status (RDSR1 or RDSR2), Erase Suspend (ERSP), Program Suspend (PGSP), Clear Status Register (CLSR), and Software Reset (RESET) commands may be accepted. ERSP and PGSP will only be accepted if memory array erase or program operations are in progress. The status register E_ERR and P_ERR bits are updated while WIP = 1. When P_ERR or E_ERR bits are set to one, the WIP bit will remain set to one indicating the device remains busy and unable to receive new operation commands. A Clear Status Register (CLSR) command must be received to return the device to standby mode. When the WIP bit is cleared to 0 no operation is in progress. This is a read-only bit.

7.5.2 Configuration Register 1 (CR1)

Related Commands: Read Configuration Register (RDCR 35h), Write Registers (WRR 01h). The Configuration Register bits can be changed using the WRR command with sixteen input cycles.

The configuration register controls certain interface and data protection functions.

Table 24. Configuration Register 1(CR1)

Bits	Field Name	Function	Type	Default State	Description
7	LC1	Latency Code	Non-Volatile	0	Selects number of initial read latency cycles See Latency Code Tables (Table 25 through Table 28)
6	LC0			0	
5	TBPROT	Configures Start of Block Protection	OTP	0	1 = BP starts at bottom (Low address) 0 = BP starts at top (High address)
4	DNU	DNU	OTP	0	Do Not Use
3	BPNV	Configures BP2-0 in Status Register	OTP	0	1 = Volatile 0 = Non-Volatile
2	TBPARM	Configures Parameter Sectors location	OTP	0	1 = 4-KB physical sectors at top, (high address) 0 = 4-KB physical sectors at bottom (Low address) RFU in uniform sector devices
1	QUAD	Puts the device into Quad I/O operation	Non-Volatile	0	1 = Quad 0 = Dual or Serial
0	FREEZE	Lock current state of BP2-0 bits in Status Register, TBPROT and TBPARM in Configuration Register, and OTP regions	Volatile	0	1 = Block Protection and OTP locked 0 = Block Protection and OTP un-locked

Latency Code (LC) CR1[7:6]: The Latency Code selects the number of mode and dummy cycles between the end of address and the start of read data output for all read commands.

Some read commands send mode bits following the address to indicate that the next command will be of the same type with an implied, rather than an explicit, instruction. The next command thus does not provide an instruction byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands.

Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system. Some read commands require additional latency cycles as the SCK frequency is increased.

Table 25 through Table 28 provide different latency settings that are configured by Cypress. The High Performance versus the Enhanced High Performance settings are selected by the ordering part number.

Where mode or latency (dummy) cycles are shown in the tables as a dash, that read command is not supported at the frequency shown. Read is supported only up to 50 MHz but the same latency value is assigned in each latency code and the command may be used when the device is operated at ≤ 50 MHz with any latency code setting. Similarly, only the Fast Read command is supported up to 133 MHz but the same 10b latency code is used for Fast Read up to 133 MHz and for the other dual and quad read commands up to 104 MHz. It is not necessary to change the latency code from a higher to a lower frequency when operating at lower frequencies where a particular command is supported. The latency code values for a higher frequency can be used for accesses at lower frequencies.

The High Performance settings provide latency options that are the same or faster than alternate source SPI memories. These settings provide mode bits only for the Quad I/O Read command.

The Enhanced High Performance settings similarly provide latency options the same or faster than additional alternate source SPI memories and adds mode bits for the Dual I/O Read, DDR Fast Read, and DDR Dual I/O Read commands.

Read DDR Data Learning Pattern (DLP) bits may be placed within the dummy cycles immediately before the start of read data, if there are 5 or more dummy cycles. See Section 9.4 Read Memory Array Commands on page 82 for more information on the DLP.

Table 25. Latency Codes for SDR High Performance

Freq. (MHz)	LC	Read		Fast Read		Read Dual Out		Read Quad Out		Dual I/O Read		Quad I/O Read	
		(03h, 13h)		(0Bh, 0Ch)		(3Bh, 3Ch)		(6Bh, 6Ch)		(BBh, BCh)		(EBh, ECh)	
		Mode	Dummy	Mode	Dummy	Mode	Dummy	Mode	Dummy	Mode	Dummy	Mode	Dummy
≤ 50	11	0	0	0	0	0	0	0	0	0	4	2	1
≤ 80	00	–	–	0	8	0	8	0	8	0	4	2	4
≤ 90	01	–	–	0	8	0	8	0	8	0	5	2	4
≤104	10	–	–	0	8	0	8	0	8	0	6	2	5
≤133	10	–	–	0	8	–	–	–	–	–	–	–	–

Table 26. Latency Codes for DDR High Performance[45]

Freq. (MHz)	LC	DDR Fast Read		DDR Dual I/O Read		Read DDR Quad I/O	
		(0Dh, 0Eh)		(BDh, BEh)		(EDh, EEh)	
		Mode	Dummy	Mode	Dummy	Mode	Dummy
≤ 50	11	0	4	0	4	1	3
≤ 66	00	0	5	0	6	1	6
≤ 66	01	0	6	0	7	1	7
≤ 66	10	0	7	0	8	1	8

Note

[45] When using DDR I/O commands with the Data Learning Pattern (DLP) enabled, a Latency Code that provides 5 or more dummy cycles should be selected to allow 1 cycle of additional time for the host to stop driving before the memory starts driving the 4 cycle DLP. It is recommended to use LC 10 for DDR Fast Read, LC 01 for DDR Dual IO Read, and LC 00 for DDR Quad IO Read, if the Data Learning Pattern (DLP) for DDR is used.

Table 27. Latency Codes for SDR Enhanced High Performance

Freq. (MHz)	LC	Read		Fast Read		Read Dual Out		Read Quad Out		Dual I/O Read		Quad I/O Read	
		(03h, 13h)		(0Bh, 0Ch)		(3Bh, 3Ch)		(6Bh, 6Ch)		(BBh, BCh)		(EBh, ECh)	
		Mode	Dummy	Mode	Dummy	Mode	Dummy	Mode	Dummy	Mode	Dummy	Mode	Dummy
≤ 50	11	0	0	0	0	0	0	0	0	4	0	2	1
≤ 80	00	–	–	0	8	0	8	0	8	4	0	2	4
≤ 90	01	–	–	0	8	0	8	0	8	4	1	2	4
≤104	10	–	–	0	8	0	8	0	8	4	2	2	5
≤133	10	–	–	0	8	–	–	–	–	–	–	–	–

Table 28. Latency Codes for DDR Enhanced High Performance[46]

Freq. (MHz)	LC	DDR Fast Read (0Dh, 0Eh)		DDR Dual I/O Read (BDh, BEh)		Read DDR Quad I/O (EDh, EEh)	
		Mode	Dummy	Mode	Dummy	Mode	Dummy
≤ 50	11	4	1	2	2	1	3
≤ 66	00	4	2	2	4	1	6
≤ 66	01	4	4	2	5	1	7
≤ 66	10	4	5	2	6	1	8
≤ 80	00	4	2	2	4	1	6
≤ 80	01	4	4	2	5	1	7
≤ 80	10	4	5	2	6	1	8

Note

46. When using DDR I/O commands with the Data Learning Pattern (DLP) enabled, a Latency Code that provides 5 or more dummy cycles should be selected to allow 1 cycle of additional time for the host to stop driving before the memory starts driving the 4 cycle DLP. It is recommended to use LC 10 for DDR Fast Read, LC 01 for DDR Dual IO Read, and LC 00 for DDR Quad IO Read, if the Data Learning Pattern (DLP) for DDR is used.

Top or Bottom Protection (TBPROT) CR1[5]: This bit defines the operation of the Block Protection bits BP2, BP1, and BP0 in the Status Register. As described in the status register section, the BP2-0 bits allow the user to optionally protect a portion of the array, ranging from 1/64, 1/4, 1/2, etc., up to the entire array. When TBPROT is set to a 0 the Block Protection is defined to start from the top (maximum address) of the array. When TBPROT is set to a 1 the Block Protection is defined to start from the bottom (zero address) of the array. The TBPROT bit is OTP and set to a 0 when shipped from Cypress. If TBPROT is programmed to 1, an attempt to change it back to 0 will fail and set the Program Error bit (P_ERR in SR1[6]).

The desired state of TBPROT must be selected during the initial configuration of the device during system manufacture; before the first program or erase operation on the main flash array. TBPROT must not be programmed after programming or erasing is done in the main flash array.

CR1[4]: Reserved for Future Use

Block Protection Non-Volatile (BPNV) CR1[3]: The BPNV bit defines whether or not the BP2-0 bits in the Status Register are volatile or non-volatile. The BPNV bit is OTP and cleared to a0 with the BP bits cleared to 000 when shipped from Cypress. When BPNV is set to a 0 the BP2-0 bits in the Status Register are non-volatile. When BPNV is set to a 1 the BP2-0 bits in the Status Register are volatile and will be reset to binary 111 after POR, hardware reset, or command reset. If BPNV is programmed to 1, an attempt to change it back to 0 will fail and set the Program Error bit (P_ERR in SR1[6]).

TBPARM CR1[2]: TBPARM defines the logical location of the parameter block. The parameter block consists of thirty-two 4-KB small sectors (SMS), which replace two 64-KB sectors. When TBPARM is set to a 1 the parameter block is in the top of the memory array address space. When TBPARM is set to a 0 the parameter block is at the Bottom of the array. TBPARM is OTP and set to a 0 when it ships from Cypress. If TBPARM is programmed to 1, an attempt to change it back to 0 will fail and set the Program Error bit (P_ERR in SR1[6]).

The desired state of TBPARM must be selected during the initial configuration of the device during system manufacture; before the first program or erase operation on the main flash array. TBPARM must not be programmed after programming or erasing is done in the main flash array.

TBPROT can be set or cleared independent of the TBPARM bit. Therefore, the user can elect to store parameter information from the bottom of the array and protect boot code starting at the top of the array, and vice versa. Or the user can select to store and protect the parameter information starting from the top or bottom together.

When the memory array is logically configured as uniform 256-KB sectors, the TBPARM bit is Reserved for Future Use (RFU) and has no effect because all sectors are uniform size.

Quad Data Width (QUAD) CR1[1]: When set to 1, this bit switches the data width of the device to 4 bit - Quad mode. That is, WP# becomes IO2 and HOLD# becomes IO3. The WP# and HOLD# inputs are not monitored for their normal functions and are internally set to HIGH (inactive). The commands for Serial, Dual Output, and Dual I/O Read still function normally but, there is no need to drive WP# and Hold# inputs for those commands when switching between commands using different data path widths. The QUAD bit must be set to one when using Read Quad Out, Quad I/O Read, Read DDR Quad I/O, and Quad Page Program commands. The QUAD bit is non-volatile.

Freeze Protection (FREEZE) CR1[0]: The Freeze Bit, when set to 1, locks the current state of the BP2-0 bits in Status Register, the TBPROT and TBPARM bits in the Configuration Register, and the OTP address space. This prevents writing, programming, or erasing these areas. As long as the FREEZE bit remains cleared to logic 0 the other bits of the Configuration Register, including FREEZE, are writable, and the OTP address space is programmable. Once the FREEZE bit has been written to a logic 1 it can only be cleared to a logic 0 by a power-off to power-on cycle or a hardware reset. Software reset will not affect the state of the FREEZE bit. The FREEZE bit is volatile and the default state of FREEZE after power-on is 0. The FREEZE bit can be set in parallel with updating other values in CR1 by a single WRR command.

7.5.3 Status Register 2 (SR2)

Related Commands: Read Status Register 2 (RDSR2 07h).

Table 29. Status Register 2 (SR2)

Bits	Field Name	Function	Type	Default State	Description
7	RFU	Reserved	–	0	Reserved for Future Use
6	RFU	Reserved	–	0	Reserved for Future Use
5	RFU	Reserved	–	0	Reserved for Future Use
4	RFU	Reserved	–	0	Reserved for Future Use
3	RFU	Reserved	–	0	Reserved for Future Use
2	RFU	Reserved	–	0	Reserved for Future Use
1	ES	Erase Suspend	Volatile, Read only	0	1 = In erase suspend mode 0 = Not in erase suspend mode
0	PS	Program Suspend	Volatile, Read only	0	1 = In program suspend mode 0 = Not in program suspend mode

Erase Suspend (ES) SR2[1]: The Erase Suspend bit is used to determine when the device is in Erase Suspend mode. This is a status bit that cannot be written. When Erase Suspend bit is set to 1, the device is in erase suspend mode. When Erase Suspend bit is cleared to 0, the device is not in erase suspend mode. Refer to Erase Suspend and Resume Commands (75h) (7Ah) for details about the Erase Suspend/Resume commands.

Program Suspend (PS) SR2[0]: The Program Suspend bit is used to determine when the device is in Program Suspend mode. This is a status bit that cannot be written. When Program Suspend bit is set to 1, the device is in program suspend mode. When the Program Suspend bit is cleared to 0, the device is not in program suspend mode. Refer to Section 9.5.4 Program Suspend (PGSP 85h) and Resume (PGRS 8Ah) on page 104 for details.

7.5.4 AutoBoot Register

Related Commands: AutoBoot Read (ABRD 14h) and AutoBoot Write (ABWR 15h).

The AutoBoot Register provides a means to automatically read boot code as part of the power-on reset, hardware reset, or software reset process.

Table 30. AutoBoot Register

Bits	Field Name	Function	Type	Default State	Description
31 to 9	ABSA	AutoBoot Start Address	Non-Volatile	000000h	512 byte boundary address for the start of boot code access
8 to 1	ABSD	AutoBoot Start Delay	Non-Volatile	00h	Number of initial delay cycles between CS# going LOW and the first bit of boot code being transferred
0	ABE	AutoBoot Enable	Non-Volatile	0	1 = AutoBoot is enabled 0 = AutoBoot is not enabled

7.5.5 Bank Address Register

Related Commands: Bank Register Access (BRAC B9h), Write Register (WRR 01h), Bank Register Read (BRRD 16h) and Bank Register Write (BRWR 17h).

The Bank Address register supplies additional high order bits of the main flash array byte boundary address for legacy commands that supply only the low order 24 bits of address. The Bank Address is used as the high bits of address (above A23) for all 3-byte address commands when EXTADD=0. The Bank Address is not used when EXTADD = 1 and traditional 3-byte address commands are instead required to provide all four bytes of address.

Table 31. Bank Address Register (BAR)

Bits	Field Name	Function	Type	Default State	Description
7	EXTADD	Extended Address Enable	Volatile	0b	1 = 4-byte (32-bits) addressing required from command. 0 = 3-byte (24-bits) addressing from command + Bank Address
6 to 1	RFU	Reserved	Volatile	00000b	Reserved for Future Use
0	BA24	Bank Address	Volatile	0	A24 for 256-Mb device, RFU for lower density device

Extended Address (EXTADD) BAR[7]: EXTADD controls the address field size for legacy SPI commands. By default (power up reset, hardware reset, and software reset), it is cleared to 0 for 3 bytes (24 bits) of address. When set to 1, the legacy commands will require 4 bytes (32 bits) for the address field. This is a volatile bit.

7.5.6 ECC Status Register (ECCSR)

Related Commands: ECC Read (ECCRD 18h). ECCSR does not have user programmable non-volatile bits. All defined bits are volatile read only status. The default state of these bits are set by hardware. See Section 9.5.1.1 Automatic ECC on page 98.

The status of ECC in each ECC unit is provided by the 8-bit ECC Status Register (ECCSR). The ECC Register Read command is written followed by an ECC unit address. The contents of the status register then indicates, for the selected ECC unit, whether there is an error in the ECC unit eight bit error correction code, the ECC unit of 16 Bytes of data, or that ECC is disabled for that ECC unit.

Table 32. ECC Status Register (ECCSR)

Bits	Field Name	Function	Type	Default State	Description
7 to 3	RFU	Reserved		0	Reserved for Future Use
2	EECC	Error in ECC	Volatile, Read only	0	1 = Single Bit Error found in the ECC unit eight bit error correction code 0 = No error.
1	EECCD	Error in ECC unit data	Volatile, Read only	0	1 = Single Bit Error corrected in ECC unit data. 0 = No error.
0	ECCDI	ECC Disabled	Volatile, Read only	0	1 = ECC is disabled in the selected ECC unit. 0 = ECC is enabled in the selected ECC unit.

ECCSR[2] = 1 indicates an error was corrected in the ECC. ECCSR[1] = 1 indicates an error was corrected in the ECC unit data. ECCSR[0] = 1 indicates the ECC is disabled. The default state of “0” for all these bits indicates no failures and ECC is enabled.

ECCSR[7:3] are reserved. These have undefined high or low values that can change from one ECC status read to another. These bits should be treated as “don’t care” and ignored by any software reading status.

7.5.7 ASP Register (ASPR)

Related Commands: ASP Read (ASPRD 2Bh) and ASP Program (ASPP 2Fh).

The ASP register is a 16-bit OTP memory location used to permanently configure the behavior of Advanced Sector Protection (ASP) features.

Table 33. ASP Register (ASPR)

Bits	Field Name	Function	Type	Default State	Description
15 to 9	RFU	Reserved	OTP	1	Reserved for Future Use
8	RFU	Reserved	OTP	Note [47]	Reserved for Future Use
7	RFU	Reserved	OTP		Reserved for Future Use
6	RFU	Reserved	OTP	1	Reserved for Future Use
5	RFU	Reserved	OTP	Note [47]	Reserved for Future Use
4	RFU	Reserved	OTP		Reserved for Future Use
3	RFU	Reserved	OTP		Reserved for Future Use
2	PWDMLB	Password Protection Mode Lock Bit	OTP	1	0 = Password Protection Mode permanently enabled. 1 = Password Protection Mode not permanently enabled.
1	PSTMLB	Persistent Protection Mode Lock Bit	OTP	1	0 = Persistent Protection Mode permanently enabled. 1 = Persistent Protection Mode not permanently enabled.
0	RFU	Reserved	OTP	1	Reserved for Future Use

Note

47. Default value depends on ordering part number, see Section 11.5 Initial Delivery State on page 139.

Reserved for Future Use (RFU) ASPR[15:3, 0].

Password Protection Mode Lock Bit (PWDMLB) ASPR[2]: When programmed to 0, the Password Protection Mode is permanently selected.

Persistent Protection Mode Lock Bit (PSTMLB) ASPR[1]: When programmed to 0, the Persistent Protection Mode is permanently selected. PWDMLB and PSTMLB are mutually exclusive, only one may be programmed to zero.

7.5.8 Password Register (PASS)

Related Commands: Password Read (PASSRD E7h) and Password Program (PASSP E8h).

Table 34. Password Register (PASS)

Bits	Field Name	Function	Type	Default State	Description
63 to 0	PWD	Hidden Password	OTP	FFFFFFFF-FFFFFFFFh	Non-volatile OTP storage of 64 bit password. The password is no longer readable after the password protection mode is selected by programming ASP register bit 2 to zero.

7.5.9 PPB Lock Register (PPBL)

Related Commands: PPB Lock Read (PLBRD A7h, PLBWR A6h).

Table 35. PPB Lock Register (PPBL)

Bits	Field Name	Function	Type	Default State	Description
7 to 1	RFU	Reserved	Volatile	00h	Reserved for Future Use
0	PPBLOCK	Protect PPB Array	Volatile	Persistent Protection Mode = 1 Password Protection Mode = 0	0 = PPB array protected until next power cycle or hardware reset 1 = PPB array may be programmed or erased.

7.5.10 PPB Access Register (PPBAR)

Related Commands: PPB Read (PPBRD E2h)

Table 36. PPB Access Register (PPBAR)

Bits	Field Name	Function	Type	Default State	Description
7 to 0	PPB	Read or Program per sector PPB	Non-volatile	FFh	00h = PPB for the sector addressed by the PPBRD or PPBP command is programmed to 0, protecting that sector from program or erase operations. FFh = PPB for the sector addressed by the PPBRD or PPBP command is erased to 1, not protecting that sector from program or erase operations.

7.5.11 DYB Access Register (DYBAR)

Related Commands: DYB Read (DYBRD E0h) and DYB Program (DYBP E1h).

Table 37. DYB Access Register (DYBAR)

Bits	Field Name	Function	Type	Default State	Description
7 to 0	DYB	Read or Write per sector DYB	Volatile	FFh	00h = DYB for the sector addressed by the DYBRD or DYBP command is cleared to 0, protecting that sector from program or erase operations. FFh = DYB for the sector addressed by the DYBRD or DYBP command is set to 1, not protecting that sector from program or erase operations.

7.5.12 SPI DDR Data Learning Registers

Related Commands: Program NVDLR (PNVDLR 43h), Write VDLR (WVDLR 4Ah), Data Learning Pattern Read (DLPRD 41h).

The Data Learning Pattern (DLP) resides in an 8-bit Non-Volatile Data Learning Register (NVDLR) as well as an 8-bit Volatile Data Learning Register (VDLR). When shipped from Cypress, the NVDLR value is 00h. Once programmed, the NVDLR cannot be reprogrammed or erased; a copy of the data pattern in the NVDLR will also be written to the VDLR. The VDLR can be written to at any time, but on reset or power cycles the data pattern will revert back to what is in the NVDLR. During the learning phase described in the SPI DDR modes, the DLP will come from the VDLR. Each IO will output the same DLP value for every clock edge. For example, if the DLP is 34h (or binary 00110100) then during the first clock edge all IO's will output 0; subsequently, the 2nd clock edge all I/O's will output 0, the 3rd will output 1, etc.

When the VDLR value is 00h, no preamble data pattern is presented during the dummy phase in the DDR commands.

Table 38. Non-Volatile Data Learning Register (NVDLR)

Bits	Field Name	Function	Type	Default State	Description
7 to 0	NVDLP	Non-Volatile Data Learning Pattern	OTP	00h	OTP value that may be transferred to the host during DDR read command latency (dummy) cycles to provide a training pattern to help the host more accurately center the data capture point in the received data bits.

Table 39. Volatile Data Learning Register (NVDLR)

Bits	Field Name	Function	Type	Default State	Description
7 to 0	VDLP	Volatile Data Learning Pattern	Volatile	Takes the value of NVDLR during POR or Reset	Volatile copy of the NVDLP used to enable and deliver the Data Learning Pattern (DLP) to the outputs. The VDLP may be changed by the host during system operation.